力积存储
ZENTEL

Z6F8GH3SCAA-MC

8 GB, 1Rx8 288-Pin DDR4-3200 UDIMM

Data Sheet

2023.06
Rev.05

8 GB DDR4 SDRAM UDIMM Specification

Specifications

Max. Speed; CAS Latency	DDR4-3200@CL=22
Row Cycle Time (tRCmin)	45.75 ns
Min. RAS-CAS-Delay (tRCD)	13.75 ns
Min. Row Precharge Time (tRP)	13.75 ns
Refresh to Active/Refresh Command Time (tRFCmin)	350 ns
Row Active Time (tRASmin)	32 ns
Operating Temperature	0 ° C to +85 °C
Storage Temperature (T_{STG})	-55 to 100 °C

Features

- 288-pin, unbuffered dual in-line memory module (UDIMM)
- 1Rx8 memory module (1 rank of x8 DDR4 SDRAMs)
- Power supply:
  - VDD = VDDQ = 1.2 V ± 5%
  - VPP = 2.5 V –5%/+10%
  - VDDSPD = 2.2 V to 3.6 V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die VREFDQ generation and calibration
- On-board I^2C serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Fly-by topology
- Terminated control command and address bus
- PCB Height: 1.23” (31.25 mm)

Ordering Information

Part Number	*Module Density*	*Configuration*	*Speed Bin (CL-nRCD-nRP)*	*Operating Temperature*	*Storage Temperature*
Z6F8GH3SCAA-MC	8 GB	1G × 64 (1Gx8 1Rank)	DDR4-3200 (22-22-22)	0℃~85℃	-55℃~100 ℃

Address Format

DIMM Density	*Row address*	*Column address*	*Device bank group address*	*Device bank address per group*	*Device configuration*	*Module rank address*	*Device Quantity*
8GB(1Rx8,X64)	64K A[15:0]	1K A[9:0]	4 BG[1:0]	4 BA[1:0]	8Gb(1Gx8)	1 CS_n[0]	8

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Pin Configurations

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	NC	145	NC	37	VSS	181	DQ29
2	VSS	146	VREFCA	38	DQ24	182	VSS
3	DQ4	147	VSS	39	VSS	183	DQ25
4	VSS	148	DQ5	40	,DM3_n, DBI3_n, NC	184	VSS
5	DQ0	149	VSS	41	NC	185	DQS3_c
6	VSS	150	DQ1	42	VSS	186	DQS3_t
7	DM0_n, DBI0_n, NC	151	VSS	43	DQ30	187	VSS
8	NC	152	DQS0_c	44	VSS	188	DQ31
9	VSS	153	DQS0_t	45	DQ26	189	VSS
10	DQ6	154	VSS	46	VSS	190	DQ27
11	VSS	155	DQ7	47	NC	191	VSS
12	DQ2	156	VSS	48	VSS	192	NC
13	VSS	157	DQ3	49	NC	193	VSS
14	DQ12	158	VSS	50	VSS	194	NC
15	VSS	159	DQ13	51	DM8_n, DBI8_n, NC	195	VSS
16	DQ8	160	VSS	52	NC	196	DQS8_c
17	VSS	161	DQ9	53	VSS	197	DQS8_t
18	DM1_n, DBI1_n, NC	162	VSS	54	NC	198	VSS
19	NC	163	DQS1_c	55	VSS	199	NC
20	VSS	164	DQS1_t	56	NC	200	VSS
21	DQ14	165	VSS	57	VSS	201	NC
22	VSS	166	DQ15	58	RESET_n	202	VSS
23	DQ10	167	VSS	59	VDD	203	CKE1
24	VSS	168	DQ11	60	CKE0	204	VDD
25	DQ20	169	VSS	61	VDD	205	RFU
26	VSS	170	DQ21	62	ACT_n	206	VDD
27	DQ16	171	VSS	63	BG0	207	BG1
28	VSS	172	DQ17	64	VDD	208	ALERT_n
29	DM2_n, DBI2_n, NC	173	VSS	65	A12	209	VDD
30	NC	174	DQS2_c	66	A9	210	A11
31	VSS	175	DQS2_t	67	VDD	211	A7
32	DQ22	176	VSS	68	A8	212	VDD
33	VSS	177	DQ23	69	A6	213	A5
34	DQ18	178	VSS	70	VDD	214	A4
35	VSS	179	DQ19	71	A3	215	VDD
36	DQ28	180	VSS	72	A1	216	A2

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
73	VDD	217	VDD	108	DQ40	252	VSS
74	CK0_t	218	CK1_t	109	VSS	253	DQ41
75	CK0_c	219	CK1_c	110	DM5_n, DBI5_n, NC	254	VSS
76	VDD	220	VDD	111	NC	255	DQS5_c
77	VSS	221	VTT	112	VSS	256	DQS5_t
KEY				113	DQ46	257	VSS
78	EVENT_n	222	PARITY	114	VSS	258	DQ47
79	A0	223	VDD	115	DQ42	259	VSS
80	VDD	224	BA1	116	VSS	260	DQ43
81	BA0	225	A10_AP	117	DQ52	261	VSS
82	RAS_n/A16	226	VDD	118	VSS	262	DQ53
83	VDD	227	RFU	119	DQ48	263	VSS
84	S0_n	228	WE_n/A14	120	VSS	264	DQ49
85	VDD	229	VDD	121	DM6_n, DBI6_n, NC	265	VSS
86	CAS_n/A15	230	Save_n,NC	122	NC	266	DQS6_c
87	ODT0	231	VDD	123	VSS	267	DQS6_t
88	VDD	232	A13	124	DQ54	268	VSS
89	S1_n	233	VDD	125	VSS	269	DQ55
90	VDD	234	A17, NC	126	DQ50	270	VSS
91	ODT1	235	C[2], NC	127	VSS	271	DQ51
92	VDD	236	VDD	128	DQ60	272	VSS
93	S2_n, C[0]	237	S3_n, C[1]	129	VSS	273	DQ61
94	VSS	238	SA2	130	DQ56	274	VSS
95	DQ36	239	VSS	131	VSS	275	DQ57
96	VSS	240	DQ37	132	DM7_n, DBI7_n, NC	276	VSS
97	DQ32	241	VSS	133	NC	277	DQS7_c
98	VSS	242	DQ33	134	VSS	278	DQS7_t
99	DM4_n, DBI4_n, NC	243	VSS	135	DQ62	279	VSS
100	NC	244	DQS4_c	136	VSS	280	DQ63
101	VSS	245	DQS4_t	137	DQ58	281	VSS
102	DQ38	246	VSS	138	VSS	282	DQ59
103	VSS	247	DQ39	139	SA0	283	VSS
104	DQ34	248	VSS	140	SA1	284	VDDSPD
105	VSS	249	DQ35	141	SCL	285	SDA
106	DQ44	250	VSS	142	VPP	286	VPP
107	VSS	251	DQ45	143	VPP	287	VPP
				144	RFU	288	VPP

Pin Descriptions

Symbol	Type	Function
CKx_t, CKx_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKEx	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CSx_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code
Cx	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14.	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
BGx	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle
BAx	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle
Ax	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses
A12/BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-thefly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
Parity	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n Low
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus

Symbol	Type	Function
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is Low, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation
DQx, CBx	I/O	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used
DQSx_t-DQSx_c	I/O	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIL_n)	I/O	Input data mask and data bus inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	Serial Data: Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input.
EVENT_n	Output	Temperature event: The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	Termination data strobe: When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component datasheet (TDQS_t and TDQS_c are not valid for UDIMMs).
VDD	Supply	Module power supply: 1.2V (TYP).
VPP	Supply	DRAM activating power supply: 2.5V –0.125V / +0.250V.
VREFCA	Supply	Reference voltage for control, command, and address pins.
VSS	Supply	Ground
VTT	Supply	Power supply for termination of address, command, and control VDD/2.
VDDSPD	Supply	Power supply used to power the I2C bus for SPD
RFU	-	Reserved for Future Use: No on DIMM electrical connection is present
NC	-	No Connect: No on DIMM electrical connection is present

General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing a total of 16 banks. Sixteen-bit-wide DDR4 SDRAM has 2 internal bank groups consisting of 4 memory banks each, providing a total of 8 banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8n-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. DDR4 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

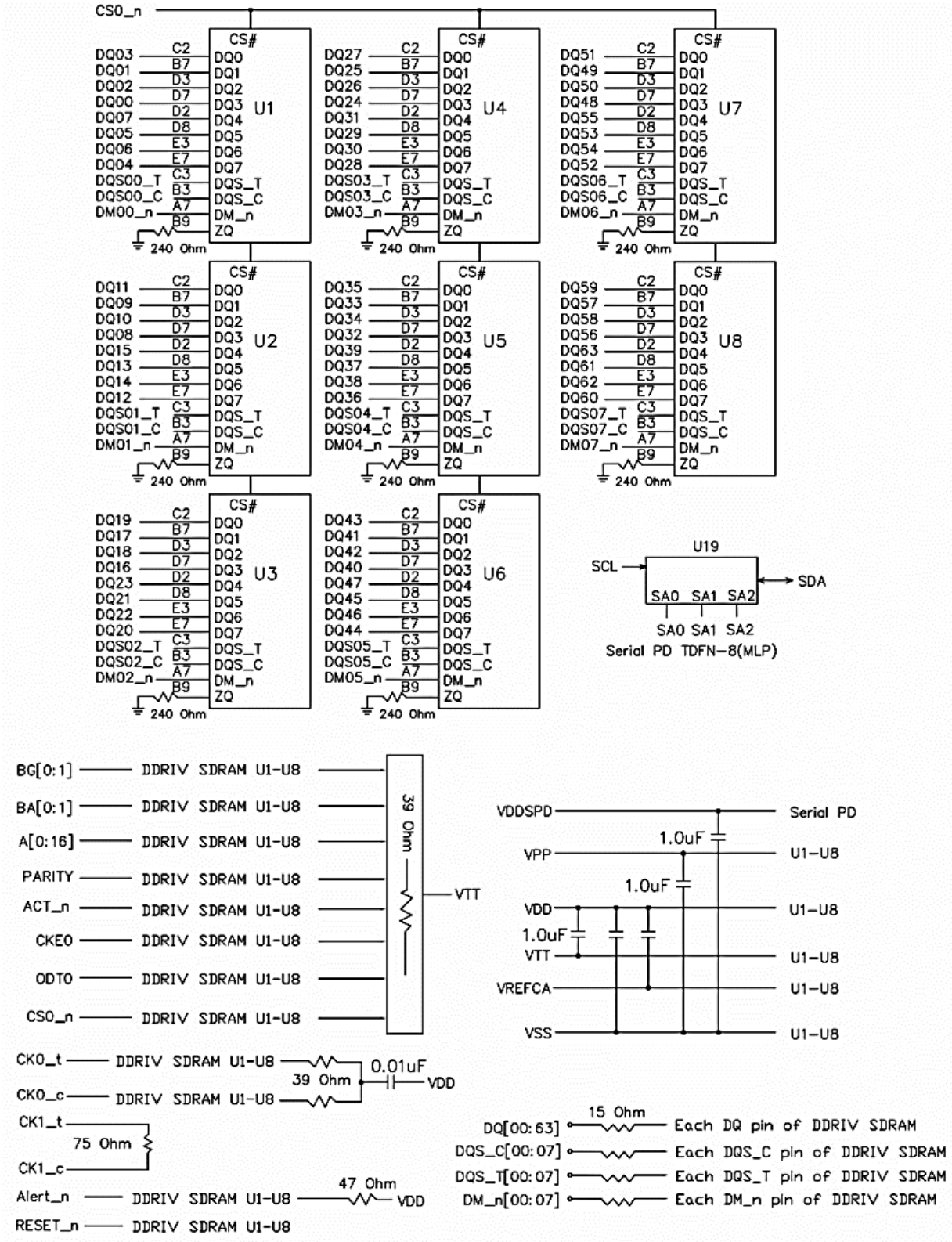
Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

Serial Presence-Detect EEPROM Operation

DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte EEPROM. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

Function Block Diagram



DQ Map

Module Pin NO.	Module DQ	Damping RES.	IC NO.	IC DQ	Module Pin NO.	Module DQ	Damping RES.	IC NO.	IC DQ
5	0	RN1(2-3)	U1	3	16	8	RN7(2-3)	U2	3
150	1	RN3(1-4)		1	161	9	RN5(1-4)		1
12	2	RN2(2-3)		2	23	10	RN8(2-3)		2
157	3	RN4(1-4)		0	168	11	RN6(1-4)		0
3	4	RN1(1-4)		7	14	12	RN7(1-4)		7
148	5	RN3(2-3)		5	159	13	RN5(2-3)		5
10	6	RN2(1-4)		6	21	14	RN8(1-4)		6
155	7	RN4(2-3)		4	166	15	RN6(2-3)		4
27	16	RN9(2-3)	U3	3	38	24	RN15(2-3)	U4	3
172	17	RN11(1-4)		1	183	25	RN13(1-4)		1
34	18	RN12(2-3)		2	45	26	RN14(2-3)		2
179	19	RN10(1-4)		0	190	27	RN16(1-4)		0
25	20	RN9(1-4)		7	36	28	RN15(1-4)		7
170	21	RN11(2-3)		5	181	29	RN13(2-3)		5
32	22	RN12(1-4)		6	43	30	RN14(1-4)		6
177	23	RN10(2-3)		4	188	31	RN16(2-3)		4
97	32	RN17(2-3)	U5	3	108	40	RN21(2-3)	U6	3
242	33	RN19(1-4)		1	253	41	RN23(1-4)		1
104	34	RN20(2-3)		2	115	42	RN24(2-3)		2
249	35	RN18(1-4)		0	260	43	RN22(1-4)		0
95	36	RN17(1-4)		7	106	44	RN21(1-4)		7
240	37	RN19(2-3)		5	251	45	RN23(2-3)		5
102	38	RN20(1-4)		6	113	46	RN24(1-4)		6
247	39	RN18(2-3)		4	258	47	RN22(2-3)		4
119	48	RN26(2-3)	U7	3	130	56	RN28(2-3)	U8	3
264	49	RN25(1-4)		1	275	57	RN30(1-4)		1
126	50	RN45(2-3)		2	137	58	RN29(2-3)		2
271	51	RN27(1-4)		0	282	59	RN31(1-4)		0
117	52	RN26(1-4)		7	128	60	RN28(1-4)		7
262	53	RN25(2-3)		5	273	61	RN30(2-3)		5
124	54	RN45(1-4)		6	135	62	RN29(1-4)		6
269	55	RN27(2-3)		4	280	63	RN31(2-3)		4

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.5	V	
T_{STG}	Storage Temperature	-55 to +100	°C	

Note: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Note
		Min	Max		
T_{CASE}	Operating Temperature	0	95	°C	1,2,3,4

Notes:

1. Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2. The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3. Above 85 °C the Auto-Refresh command interval has to be reduced to tREFI= 3.9 µs
4. When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”.

Operating Conditions

Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.14	1.2	1.26	V	1,2,3
Supply Voltage for Output	V_{DDQ}	1.14	1.2	1.26	V	1,2,3
Peak-to-Peak Voltage	V_{PP}	2.375	2.5	2.75	V	3
Reference Voltage for ADD, CMD inputs	V_{REF}	0.49 ×V_{DD}	0.5 ×V_{DDQ}	0.51 ×V_{DD}	V	

Notes:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

Single-ended AC & DC input levels for Command and Address

Parameter	Symbol	Min.	Max.	Unit
$V_{IH.CA}$(DC65)	DC input logic high	V_{REFCA} + 0.065	V_{DD}	V
$V_{IL.CA}$(DC65)	DC input logic low	V_{SS}	V_{REFCA}-0.065	V
$V_{IH.CA}$(AC90)	AC input logic high	V_{SS}+0.09		V
$V_{IL.CA}$(AC90)	AC input logic low		V_{REF}-0.09	V

I_{DD}/I_{PP} Specifications and Conditions

Symbol	Description
IDD0 IPP0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD1 IPP1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2N IPP2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2P IPP2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD3N IPP3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern
IDD3P IPP3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD4R IPP4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[2] ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4W IPP4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks:

Symbol	Description
	0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5B IPP5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5F2 IPP5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2,
IDD5F4 IPP5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4,
IDD6N IPP6N	Self Refresh Current: Normal Temperature Range Tcase: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MIDLEVEL
IDD6E IPP6E	Self-Refresh Current: Extended Temperature Range) TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD6R IPP6R	Self-Refresh Current: Reduced Temperature Range TCase: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced[4] ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: MID-LEVEL
IDD6A IPP6A	Auto Self-Refresh Current TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto[4] ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: MID-LEVEL
IDD7 IPP7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD8 IPP8	Maximum Power Down Current TBD

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable - set MR1 [A12 = 0] : Qoff = Output buffer enabled - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7 RTT_Nom enable - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6 RTT_WR enable - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2 RTT_PARK disable - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s 010] : 1866MT/s, 2133MT/s 011] : 2400MT/s Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate DLL disabled : set MR1 [A0 = 0] CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s 010] : 2400MT/s Read DBI enabled : set MR5 [A12 = 1] Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal 01] : Reduced Temperature range 10] : Extended Temperature range 11] : Auto Self Refresh

I_{DD} Specification

Product Type	Z6F8GH3SCAA-MC	Unit	Note
Organization	8GB		
	1 Rank (X8)		
	X64		
Symbol	Current		
IDD0	296	mA	2
IDD1	369	mA	2
IDD2N	240	mA	3
IDD2NT	280	mA	2
IDD2P	168	mA	3
IDD2Q	200	mA	3
IDD3N	264	mA	3
IDD3P	208	mA	3
IDD4R	1056	mA	2
IDD4W	968	mA	2
IDD5B	1632	mA	2
IDD5F2	1176	mA	2
IDD5F4	1056	mA	2
IDD6N	168	mA	3
IDD6E	224	mA	3
IDD6R	112	mA	3
IDD6A	224	mA	3
IDD7	1200	mA	2
IDD8	96	mA	3

Notes:

1. Calculated values from Device data.
2. One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
3. All ranks in this IDD/IPP condition

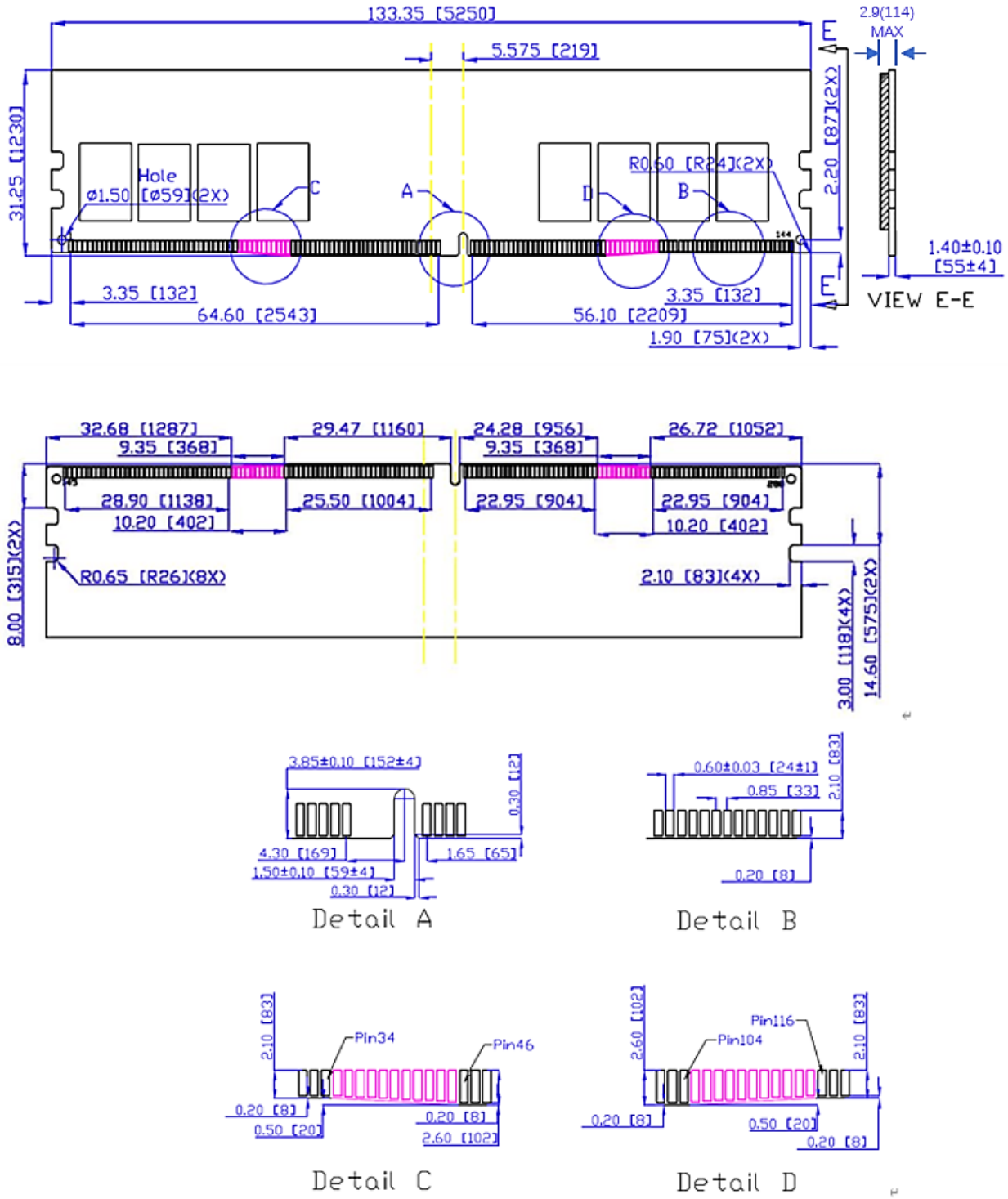
I_{PP} Specification

Product Type	Z6F8GH3SCAA-MC	Unit	Note
Organization	8GB		
	1 Rank (X8)		
	X64		
Symbol	Current		
IPP0	40	mA	2
IPP1	48	mA	2
IPP2N	25.6	mA	3
IPP2P	25	mA	3
IPP3N	128	mA	3
IPP3P	128	mA	3
IPP4R	153	mA	2
IPP4W	153	mA	2
IPP5B	488	mA	2
IPP6N	320	mA	3
IPP6E	265	mA	3
IPP6R	40	mA	3
IPP6A	56	mA	3
IPP7	32.8	mA	2
IPP8	56	mA	3

Notes:
1. Calculated values from Device data.
2. One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
3. All ranks in this IDD/IPP condition

Module Dimensions

All dimensions are in millimeter[mils] and should be kept within a tolerance of +/- 0.15[6], unless otherwise specified.



Change History			
Document No.: DSZ6F8GH3SCAAZF.(Rev.#)			
Rev. #	**Who**	**When**	**What**
01	SAE	2022-12-23	Initial version derived from DSA6F8GH3SBAAMCZF.04; Updated logo
02	Rik	2023-02-28	Add physical image Add Ordering Information
03	SAE	2023-03-07	Add IDD&IPP Specification, IDD/IPP Specifications and Conditions, Address Format, Pin Configurations, Pin Descriptions, Operating Conditions, DQ Map and Function Block Diagrams
04	Rik	2023-04-14	Updated Pin Configurations
05	Rik	2023-06	Updated Module Dimensions