力积存储
ZENTEL

Z6FBGH3DBPA-ME

32 GB, 2Rx8 288-Pin DDR4-3200 RDIMM

Data Sheet

2023.06
Rev.01

32 GB DDR4 SDRAM RDIMM Specification

Specifications

Max. Speed; CAS Latency	DDR4-3200@CL=22
Row Cycle Time (tRC min)	45.75 ns
Refresh to Active/Refresh Command Time (tRFC min)	350 ns
RAS-CAS-Delay (tRCD min)	13.75 ns
Row Precharge Time (tRP min)	13.75 ns
Row Active Time (tRAS min)	32 ns
tCK(min)	0.625 ns
Operating Temperature	0 °C to +95 °C
Storage Temperature (T_{STG})	-55 °C to 100 °C

Features

- 288-pin, Registered dual in-line memory module (RDIMM)
- 2Rx8 memory module (2 rank of x8 DDR4 SDRAMs)
- Power supply:
  - VDD = VDDQ = 1.2 V ± 5%
  - VPP = 2.5 V –5%/+10%
  - VDDSPD = 2.5 V ± 10 %
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- Internal V_{REFDQ} generation and calibration
- On-board I^2C serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Fly-by topology
- Terminated control command and address bus
- PCB Height: 1.23” (31.25 mm)

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Address Format

DIMM Density	*Row address*	*Column address*	*Device bank group address*	*Device bank address per group*	*Device configuration*	*Module rank address*	*Device Quantity*
32GB(2Rx8,X72)	128K A[16:0]	1K A[9:0]	4 BG[1:0]	4 BA[1:0]	16Gb(2Gx8)	1 CS_n[1:0]	18

Pin Configurations

Front Side Pin		Back Side Pin		Front Side Pin		Back Side Pin	
Symbol	Pin	Pin	Symbol	Symbol	Pin	Pin	Symbol
NC	1	145	NC	CK0_t	74	218	CK1_t
VSS	2	146	VREFCA	CK0_c	75	219	CK1_c
DQ4	3	147	VSS	VDD	76	220	VDD
VSS	4	148	DQ5	VTT	77	221	VTT
DQ0	5	149	VSS	KEY			
VSS	6	150	DQ1				
TDQS9_t,DQS9_t,DM0_n,DBI0_n,NC	7	151	VSS	EVENT_n	78	222	PARITY
TDQS9_c, DQS9_c, NC	8	152	DQS0_c	A0	79	223	VDD
VSS	9	153	DQS0_t	VDD	80	224	BA1
DQ6	10	154	VSS	BA0	81	225	A10/AP
VSS	11	155	DQ7	RAS_n/A16	82	226	VDD
DQ2	12	156	VSS	VDD	83	227	RFU
VSS	13	157	DQ3	CS0_n	84	228	WE_n/A14
DQ12	14	158	VSS	VDD	85	229	VDD
VSS	15	159	DQ13	CAS_n/A15	86	230	NC,SAVE_n
DQ8	16	160	VSS	ODT0	87	231	VDD
VSS	17	161	DQ9	VDD	88	232	A13
TDQS10_t, DQS10_t, DM1_n, DBI1_n, NC	18	162	VSS	CS1_n	89	233	VDD
TDQS10_c, DQS10_c, NC	19	163	DQS1_c	VDD	90	234	NC,A17
VSS	20	164	DQS1_t	ODT1	91	235	NC,C2
DQ14	21	165	VSS	VDD	92	236	VDD
VSS	22	166	DQ15	C0, CS2_n,NC	93	237	NC, CS3_n, C1
DQ10	23	167	VSS	VSS	94	238	SA2
VSS	24	168	DQ15	DQ36	95	239	VSS
DQ20	25	169	VSS	VSS	96	240	DQ37
VSS	26	170	DQ11	DQ32	97	241	VSS
DQ16	27	171	VSS	VSS	98	242	DQ33
VSS	28	172	DQ17	TDQS13_t, DQS13_t, DM4_n, DBI4_n, NC	99	243	VSS
TDQS11_t, DQS11_t, DM2_n, DBI2_n, NC	29	173	VSS	TDQS13_c, DQS13_c, NC	100	244	DQS4_c
TDQS11_c, DQS11_c, NC	30	174	DQS2_c	VSS	101	245	DQS4_t
VSS	31	175	DQS2_t	DQ38	102	246	VSS
DQ22	32	176	VSS	VSS	103	247	DQ39
VSS	33	177	DQ23	DQ34	104	248	VSS
DQ18	34	178	VSS	VSS	105	249	DQ35
VSS	35	179	DQ19	DQ44	106	250	VSS
DQ28	36	180	VSS	VSS	107	251	DQ45
VSS	37	181	DQ29	DQ40	108	252	VSS
DQ24	38	182	VSS	VSS	109	253	DQ41
VSS	39	183	DQ25	TDQS14_t, DQS14_t, DM5_n, DBI5_n, NC	110	254	VSS
TDQS12_t, DQS12_t, DM3_n, DBI3_n, NC	40	184	VSS	TDQS114_c, DQS14_c, NC	111	255	DQS5_c
TDQS12_c, DQS12_c, NC	41	185	DQS3_c	VSS	112	256	DQS5_t

Front Side Pin		Back Side Pin		Front Side Pin		Back Side Pin	
Symbol	Pin	Pin	Symbol	Symbol	Pin	Pin	Symbol
VSS	42	186	DQS3_t	DQ46	113	257	VSS
DQ30	43	187	VSS	VSS	114	258	DQ47
VSS	44	188	DQ31	DQ42	115	259	VSS
DQ26	45	189	VSS	VSS	116	260	DQ43
VSS	46	190	DQ27	DQ52	117	261	VSS
CB4,NC	47	191	VSS	VSS	118	262	DQ53
VSS	48	192	CB5,NC	DQ48	119	263	VSS
CB0,NC	49	193	VSS	VSS	120	264	DQ49
VSS	50	194	CB1,NC	TDQS15_t, DQS15_t, DM6_n, DBI6_n, NC	121	265	VSS
TDQS17_t, DQS17_t, DM8_n, DBI8_n, NC	51	195	VSS	TDQS115_c, DQS15_c, NC	122	266	DQS6_c
TDQS117_c, DQS17_c, NC	52	196	DQS8_c	VSS	123	267	DQS6_t
VSS	53	197	DQS8_t	DQ54	124	268	VSS
CB6,NC	54	198	VSS	VSS	125	269	DQ55
VSS	55	199	CB7,NC	DQ50	126	270	VSS
CB2,NC	56	200	VSS	VSS	127	271	DQ51
VSS	57	201	CB3,NC	DQ60	128	272	VSS
RESET_n	58	202	VSS	VSS	129	273	DQ61
VDD	59	203	CKE1	DQ56	130	274	VSS
CKE0	60	204	VDD	VSS	131	275	DQ57
VDD	61	205	RFU	TDQS16_t, DQS16_t, DM7_n, DBI6_n, NC	132	276	VSS
ACT_n	62	206	VDD	TDQS116_c, DQS16_c, NC	133	277	DQS7_c
BG0	63	207	BG1	VSS	134	278	DQS7_t
VDD	64	208	ALERT_n	DQ62	135	279	VSS
A12/BC_n	65	209	VDD	VSS	136	280	DQ63
A9	66	210	A11	DQ58	137	281	VSS
VDD	67	211	A7	VSS	138	282	DQ59
A8	68	212	VDD	SA0	139	283	VSS
A6	69	213	A5	SA1	140	284	VDDSPD
VDD	70	214	A4	SCL	141	285	SDA
A3	71	215	VDD	VPP	142	286	VPP
A12/BC_n	72	216	A2	VPP	143	287	VPP
VDD	73	217	VDD	RFU	144	288	VPP

Pin Descriptions

Symbol	Type	Function
CKx_t, CKx_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKEx	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CSx_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code
Cx	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODTx	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14.	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
BGx	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle
BAx	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle
Ax	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses
A12/BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-thefly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
PAR	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n Low
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus

Symbol	Type	Function
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is Low, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation
DQx, CBx	I/O	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used
DQSx_t-DQSx_c	I/O	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIL_n)	I/O	Input data mask and data bus inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for SODIMMs).
SDA	I/O	Serial Data: Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input.
EVENT_n	Output	Temperature event: The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	Termination data strobe: When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component datasheet (TDQS_t and TDQS_c are not valid for SODIMMs).
VDD	Supply	Module power supply: 1.2V (TYP).
VPP	Supply	DRAM activating power supply: 2.5V –0.125V / +0.250V.
VREFCA	Supply	Reference voltage for control, command, and address pins.
VSS	Supply	Ground
VTT	Supply	Power supply for termination of address, command, and control VDD/2.
VDDSPD	Supply	Power supply used to power the I2C bus for SPD
RFU	-	Reserved for Future Use: No on DIMM electrical connection is present
NC	-	No Connect: No on DIMM electrical connection is present

General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing a total of 16 banks. Sixteen-bit-wide DDR4 SDRAM has 2 internal bank groups consisting of 4 memory banks each, providing a total of 8 banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8n-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. DDR4 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

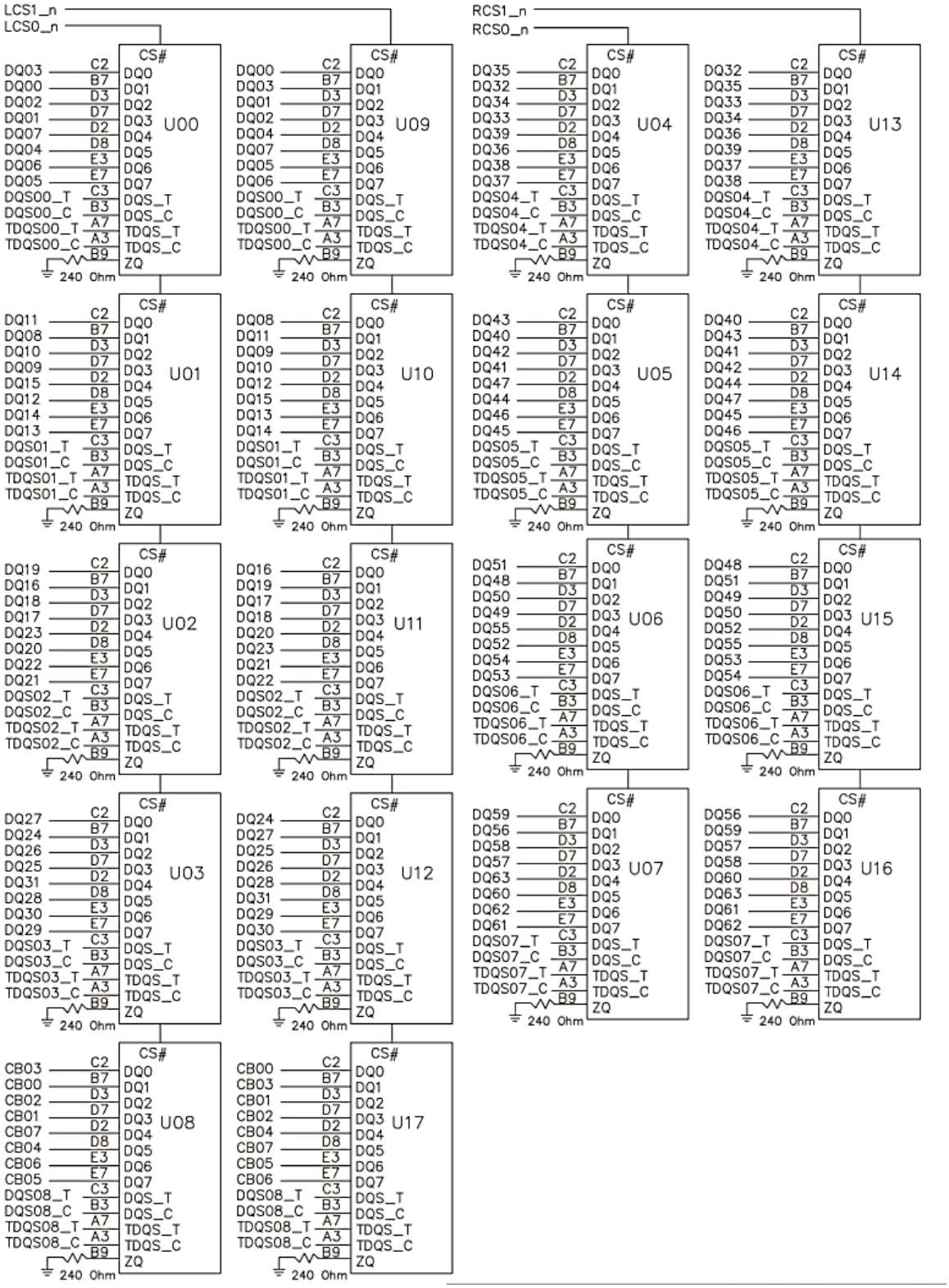
Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

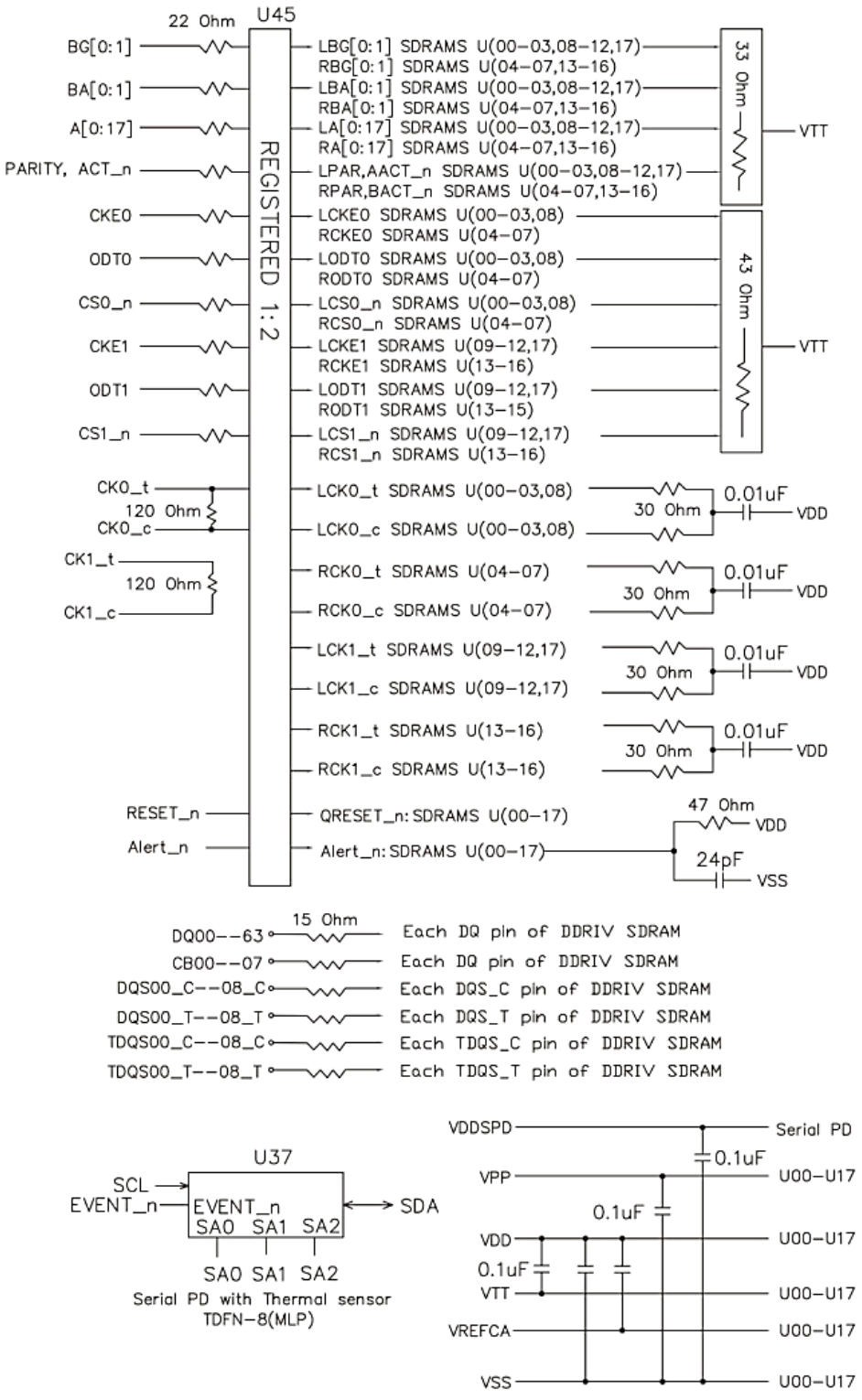
Serial Presence-Detect EEPROM Operation

DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte EEPROM. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM’s SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

Function Block Diagram



Function Block Diagram -2



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.5	V	
T_{STG}	Storage Temperature	-55 to +100	°C	

Note: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Note
		Min	Max		
T_{CASE}	Operating Temperature	0	95	°C	1,2,3,4

Notes:

1. Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2. The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
3. Above 85 °C the Auto-Refresh command interval has to be reduced to tREFI= 3.9 µs
4. When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”.

Operating Conditions

Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.14	1.2	1.26	V	1,2,3
Supply Voltage for Output	V_{DDQ}	1.14	1.2	1.26	V	1,2,3
Peak-to-Peak Voltage	V_{PP}	2.375	2.5	2.75	V	3
Reference Voltage for ADD, CMD inputs	V_{REF}	0.49 ×V_{DD}	0.5 ×V_{DDQ}	0.51 ×V_{DD}	V	

Notes:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. DC bandwidth is limited to 20MHz.

Single-ended AC & DC input levels for Command and Address

Parameter	Symbol	Min.	Max.	Unit
$V_{IH.CA}$(DC65)	DC input logic high	V_{REFCA} + 0.065	V_{DD}	V
$V_{IL.CA}$(DC65)	DC input logic low	V_{SS}	V_{REFCA}-0.065	V
$V_{IH.CA}$(AC90)	AC input logic high	V_{SS}+0.09		V
$V_{IL.CA}$(AC90)	AC input logic low		V_{REF}-0.09	V

I_{DD}/I_{PP} Specifications and Conditions

Symbol	Description
IDD0 IPP0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD1 IPP1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2N IPP2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2P IPP2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1]; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD3N IPP3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern
IDD3P IPP3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD4R IPP4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[2] ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4W IPP4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks:

Symbol	Description
	0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5B IPP5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5F2 IPP5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2,
IDD5F4 IPP5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4,
IDD6N IPP6N	Self Refresh Current: Normal Temperature Range Tcase: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MIDLEVEL
IDD6E IPP6E	Self-Refresh Current: Extended Temperature Range) TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD6R IPP6R	Self-Refresh Current: Reduced Temperature Range TCase: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced[4] ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: MID-LEVEL
IDD6A IPP6A	Auto Self-Refresh Current TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto[4] ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: MID-LEVEL
IDD7 IPP7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD8 IPP8	Maximum Power Down Current TBD

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable - set MR1 [A12 = 0] : Qoff = Output buffer enabled - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7 RTT_Nom enable - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6 RTT_WR enable - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2 RTT_PARK disable - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s 010] : 1866MT/s, 2133MT/s 011] : 2400MT/s Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate DLL disabled : set MR1 [A0 = 0] CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s 010] : 2400MT/s Read DBI enabled : set MR5 [A12 = 1] Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal 01] : Reduced Temperature range 10] : Extended Temperature range 11] : Auto Self Refresh

I_{DD} Specification

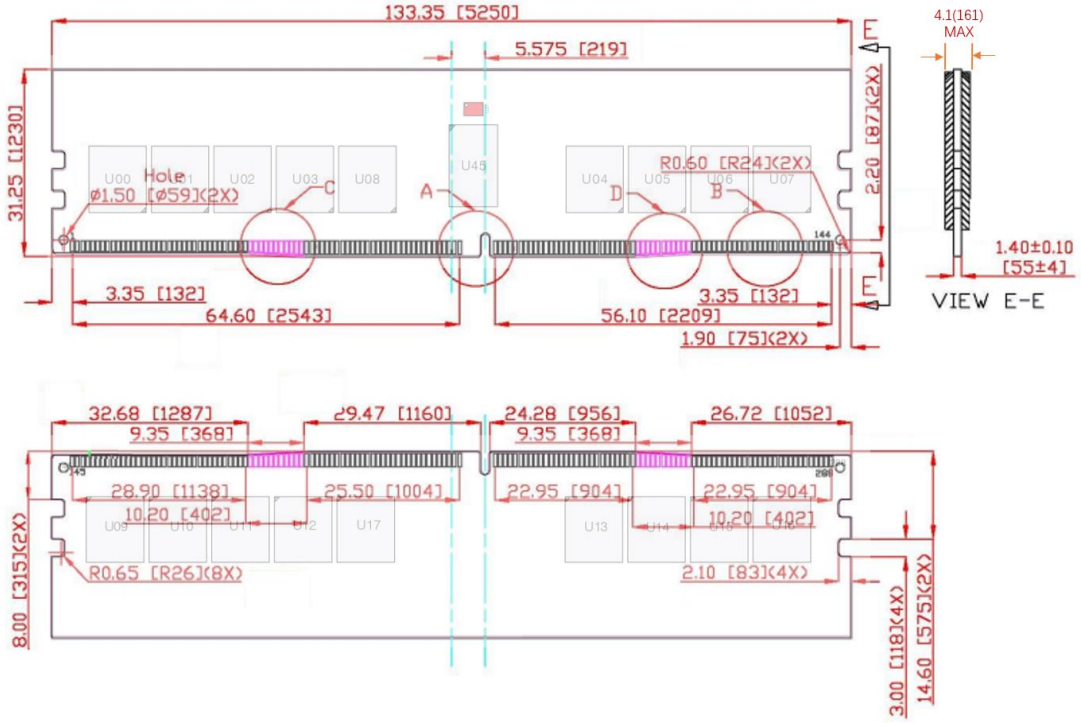
Product Type	Z6FBGH3DBPA-ME	Unit
Organization	32 GB	
	2 Rank (X8)	
	X72	
Symbol	Current	
IDD0	828	mA
IDD0A	828	mA
IDD1	972	mA
IDD1A	1044	mA
IDD2N	648	mA
IDD2NA	648	mA
IDD2NT	720	mA
IDD2NL	468	mA
IDD2NG	648	mA
IDD2ND	594	mA
IDD2N_par	666	Ma
IDD2P	468	mA
IDD2Q	612	mA
IDD3N	1332	mA
IDD3NA	1332	mA
IDD3P	1170	mA
IDD4R	2682	mA
IDD4RA	2736	mA
IDD4RB	2718	
IDD4W	2574	mA
IDD4WA	2664	mA
IDD4WB	2430	mA
IDD4WC	2574	mA
IDD5B	3042	mA
IDD5F2	10422	mA
IDD5F4	7182	mA
IDD6N	5958	mA
IDD6E	846	mA
IDD6R	1260	mA
IDD6A	396	mA
IDD7	1386	mA
IDD8	2880	mA

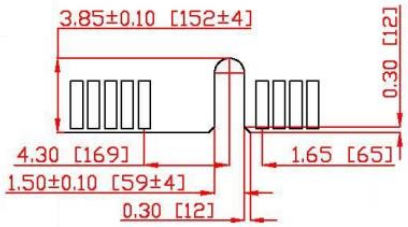
I_{PP} Specification

Product Type	Z6FBGH3DBPA-ME	Unit
Organization	32 GB	
	2 Rank (X8)	
	X72	
Symbol	Current	
IPP0	57.6	mA
IPP1	63	mA
IPP2N	34.2	mA
IPP2P	34.2	mA
IPP3N	39.6	mA
IPP3P	39.6	mA
IPP4R	93.6	mA
IPP4W	93.6	mA
IPP5B	1026	mA
IPP5F2	720	mA
IPP5F4	594	mA
IPP6N	86.4	mA
IPP6E	136.8	mA
IPP6R	52.2	mA
IPP6A	120.6	mA
IPP7	273.6	mA
IPP8	34.2	mA

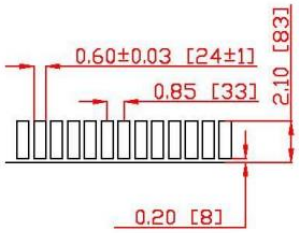
Module Dimensions

All dimensions are in millimeter[mils] and should be kept within a tolerance of +/- 0.15[6], unless otherwise specified.

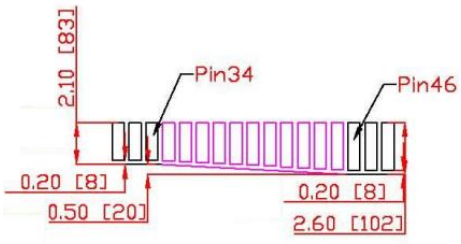




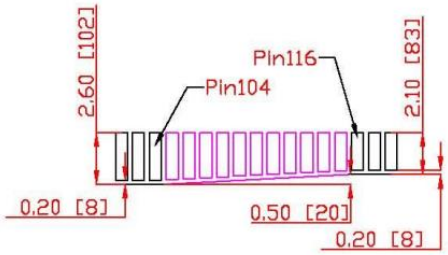
Detail A



Detail B



Detail C



Detail D

Change History			
Document No.: DSZ6FBGH3DBPAZF.(Rev.#)			
Rev. #	**Who**	**When**	**What**
01	Rik	2023-06	Initial version