力积存储
ZENTEL

Z6T8GZ3DAAA-GE

8 GB, 2Rx8 240-Pin DDR3-1600 UDIMM

Data Sheet

2023.04
Rev.01

8 GB DDR3 SDRAM UDIMM Specification

Specifications

Max. Speed	DDR3-1600
Fast Data Transfer Rates	PC3-12800
tRAS (min) (ns)	35
tRCD (min) (ns)	13.75
tRP (min) (ns)	13.75
tRC (min) (ns)	48.75
CL-tRCD-tRP	11-11-11
Operating Temperature (° C)	0 to +70

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- 2Rx8 memory module (2 rank of x8 DDR3 SDRAMs)
- Power supply:
  - VDD = 1.5V(1.425~1.575V)
  - VDDSPD = 3.0 V to 3.6 V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- On-board I^2C serial presence-detect (SPD) EEPROM
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Fly-by topology
- Module height: 1.181” (30.00 mm)
- Gold edge contacts
- Terminated control, command, and address bus

Pin Assignments (Front side/back side)

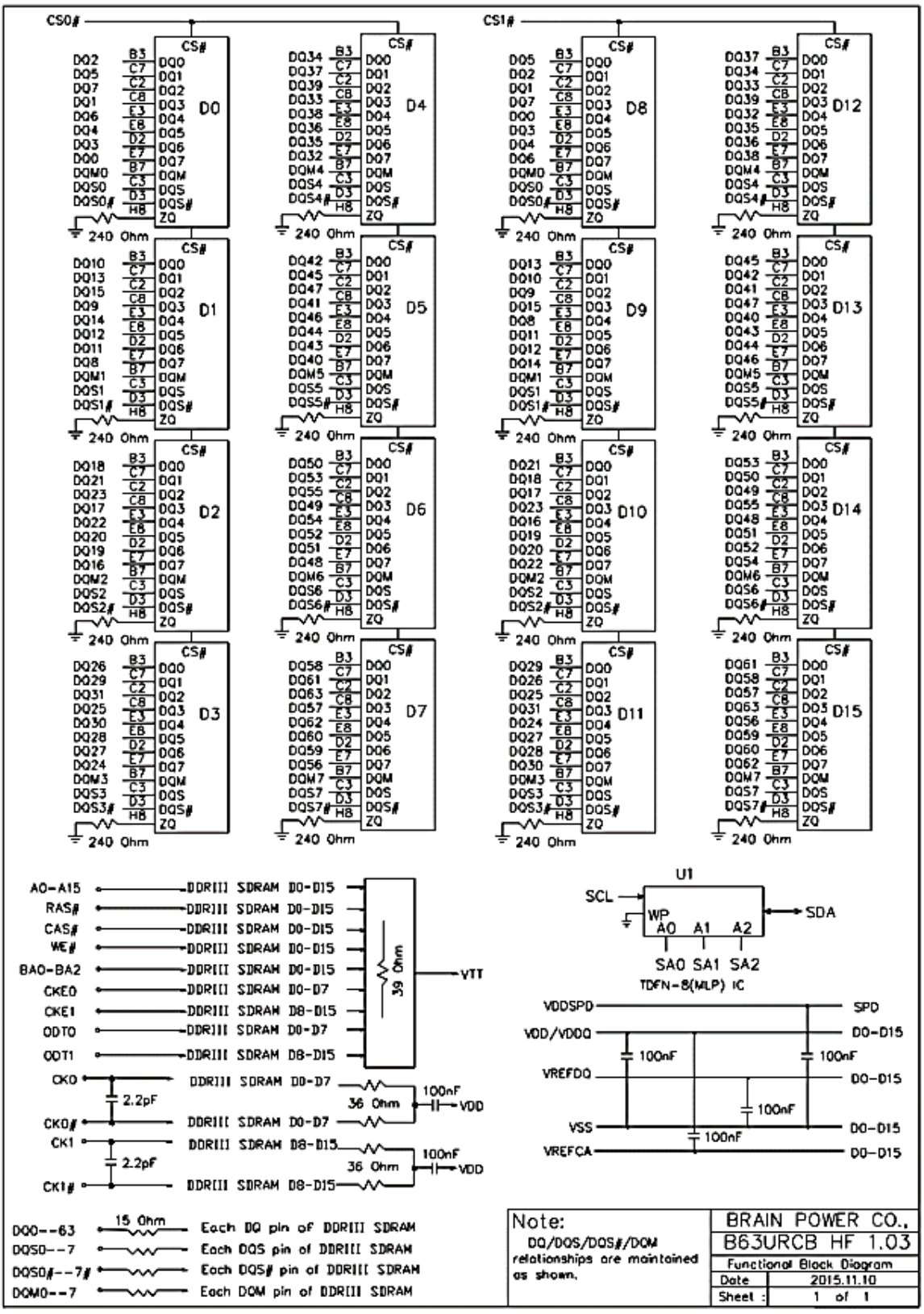
Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREFDQ	42	NC	82	DQ33	121	VSS	162	NC	202	VSS
2	VSS	43	NC	83	VSS	122	DQ4	163	VSS	203	DM4,DQS13
3	DQ0	44	VSS	84	DQS4#	123	DQ5	164	NC	204	DQS13#
4	DQ1	45	NC	85	DQS4	124	VSS	165	NC	205	VSS
5	VSS	46	NC	86	VSS	125	DM0,DQS9	166	VSS	206	DQ38
6	DQS0#	47	VSS	87	DQ34	126	NC,DQS9#	167	Test	207	DQ39
7	DQS0	48	NC	88	DQ35	127	VSS	168	Reset	208	VSS
8	VSS	KEY		89	VSS	128	DQ6	KEY		209	DQ44
9	DQ2	49	NC	90	DQ40	129	DQ7	169	CKE1	210	DQ45
10	DQ3	50	CKE0	91	DQ41	130	VSS	170	VDD	211	VSS
11	VSS	51	VDD	92	VSS	131	DQ12	171	A15	212	DM5,DQS14
12	DQ8	52	BA2	93	DQS5#	132	DQ13	172	A14	213	DQS14#
13	DQ9	53	NC	94	DQS5	133	VSS	173	VDD	214	VSS
14	VSS	54	VDD	95	VSS	134	DM1,DQS10	174	A12	215	DQ46
15	DQS1#	55	ALL	96	DQ42	135	NC,DQS10#	175	A9	216	DQ47
16	DQS1	56	A7	97	DQ43	136	VSS	176	VDD	217	VSS
17	VSS	57	VDD	98	VSS	137	DQ14	177	A8	218	DQ52
18	DQ10	58	A5	99	DQ48	138	DQ15	178	A6	219	DQ53
19	DQ11	59	A4	100	DQ49	139	VSS	179	VDD	220	VSS
20	VSS	60	VDD	101	VSS	140	DQ20	180	A3	221	DM6,DQS15
21	DQ16	61	A2	102	DQS6#	141	DQ21	181	A1	222	DQS15#
22	DQ17	62	VDD	103	DQS6	142	VSS	182	VDD	223	VSS
23	VSS	63	CK1	104	VSS	143	DQS11	183	VDD	224	DQ54
24	DQS2#	64	CK1#	105	DQ50	144	DQS11#	184	CK0	225	DQ55
25	DQS2	65	VDD	106	DQ51	145	VSS	185	CK0#	226	VSS
26	VSS	66	VDD	107	VSS	146	DQ22	186	VDD	227	DQ60
27	DQ18	67	VREFCA	108	DQ56	147	DQ23	187	Free	228	DQ61
28	DQ19	68	NC, Par-In	109	DQ57	148	VSS	188	A0	229	VSS
29	VSS	69	VDD	110	VSS	149	DQ28	189	VDD	230	DM7,DQS16
30	DQ24	70	A10	111	DQS7#	150	DQ29	190	BA1/ BA0	231	DQS16#
31	DQ25	71	BA0/BA1	112	DQS7	151	VSS	191	VDD	232	VSS
32	VSS	72	VDD	113	VSS	152	DM3/DQS12	192	RAS#	233	DQ62
33	DQS3#	73	WE#	114	DQ58	153	DQS12#	193	S0#	234	DQ63
34	DQS3	74	CAS#	115	DQ59	154	VSS	194	VDD	235	VSS
35	VSS	75	VDD	116	VSS	155	DQ30	195	ODT0	236	VDDSPD
36	DQ26	76	S1#	117	SA0	156	DQ31	196	A13	237	SA1
37	DQ27	77	ODT1	118	SCL	157	VSS	197	VDD	238	SDA
38	VSS	78	VDD	119	SA2	158	NC	198	Free	239	VSS
39	NC	79	RFU SPD#	120	VTT	159	NC	199	VSS	240	VTT
40	NC	80	VSS			160	VSS	200	DQ36		
41	VSS	81	DQ32			161	NC	201	DQ37		

Pin Descriptions

Pin Name	Function
A0~A15	SDRAM address bus
BA0~BA2	SDRAM bank select
RAS#	SDRAM row address strobe
CAS#	SDRAM column address strobe
WE#	SDRAM write enable
S0#	DIMM Rank Select Lines
CKE0	SDRAM clock enable lines
ODT0	On-die termination control lines
DQ0-DQ63	DIMM memory data bus
DQS0~DQS7	SDRAM data strobes(positive line of differential pair)
DQS0#~DQS7#	SDRAM data strobes(negative line of differential pair)
DM0 ~DM7	SDRAM data masks high data strobes(x8-based X64 DIMMs)
CK0-CK1	SDRAM clocks(positive line of differential pair)
CK0#-CK1#	SDRAM clocks(negative line of differential pair)
SCL	I^2C serial bus clock for EEPROM
SDA	I^2C serial bus data line for EEPROM
SA0-SA1	I^2C slave address select for EEPROM
VDD*	SDRAM core power supply
VDDQ*	SDRAM I/0 Driver power supply
VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return(ground)
VDDSPD	Serial EEPROM positive power supply
NC	Spare pins(no connect)
TEST	Used by memory bus analysis tools(unused on memory DIMMS)
RESET	Set DRAMs to Known State
NF	No function
VTT	SDRAM I/O termination supply
RSVD	Reserved for future use
EVENT#	An output of the thermal sensor to indicate critical module temperature

*VDD and VDDQ pins are tied common to a single power-plane on these designs.

Functional Diagram



General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins. DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Serial Presence-Detect EEPROM Operation

The 2K-bit Serial Presence Detect (SPD) EEPROM is fully compatible to industrial standard I2C/SMBus interface and compliant to the JEDEC 42.4 specification. The EEPROM memory is organized as 256 x 8 bits. This is designed for memory module applications in most PC and Server platforms, as well as other related applications. The EEPROM operates from 1.7V to 3.6V and is offered in 8-pin Ultra-thin DFN package, 2 mm x 3 mm x 0.6 mm (max.), which is lead-free, RoHS, halogen free or Green compliance, providing space as well as cost saving for DIMM manufactures.

One of the features is to permanently lock the data in its first half (lower) 128 bytes (address 00h to 7Fh). This feature is specifically designed for use in DRAM DIMM with SPD. All information concerning the DRAM module configuration (e.g. access speed, size, and organization) can be kept write-protected in the first half of the memory. The second half (upper) 128 bytes of the memory (address 80h to FFh) can't be write-protected using two different software write protection mechanisms. By sending a specified sequence to the device, the first 128 bytes memory can be write-protected either permanently or resettable. The operating ambient temperature range is from -40°C to +85°C.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.975	V	1, 2
Power supply voltage for output	VDDQ	-0.4 to +1.975	V	1, 2
Input voltage	VIN	-0.4 to +1.975	V	1
Output voltage	VOUT	-0.4 to +1.975	V	1

Notes:

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions for DDR3 (1.5V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1, 2
Input reference voltage command/address bus	VREFCA(DC)	0.49*VDD	0.5*VDD	0.51*VDD	V	
I/O reference voltage DQ bus	VREFDQ(DC)	0.49*VDD	0.5*VDD	0.51*VDD	V	
Module ambient operating temperature	TA	0	-	70	°C	3
DDR3 SDRAM component case operating temperature	TC	0	-	95	°C	4

Notes:

1. If minimum limit is exceeded, input levels shall be governed by DDR3 specifications.
2. Under 1.5V operation, the DDR3 device operates to the DDR3 specification under the same speed timings as defined for this device.
3. TA and TC are simultaneous requirements.
4. The refresh rate is required to double when 85°C < TC ≤ 95°C.

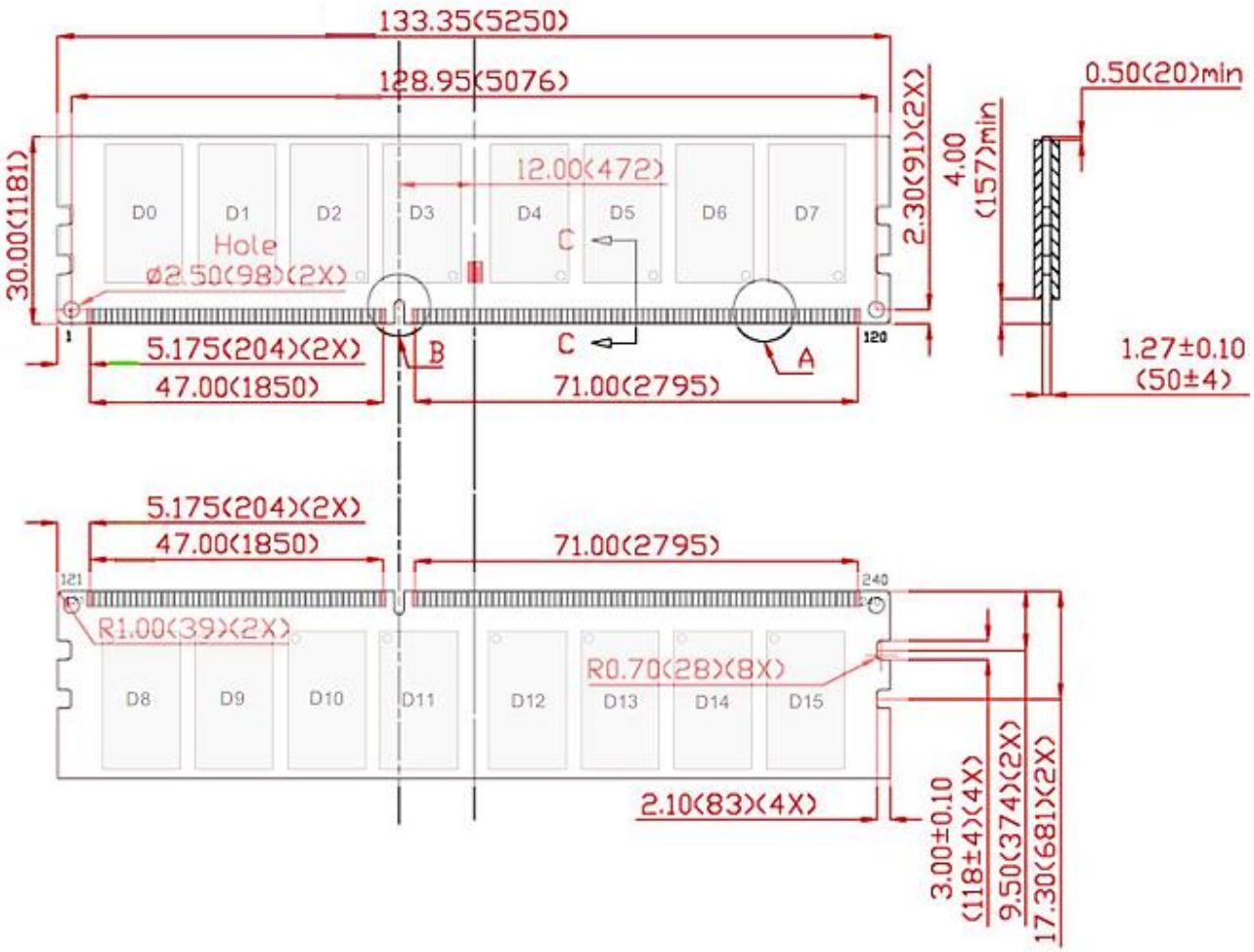
IDD Specifications

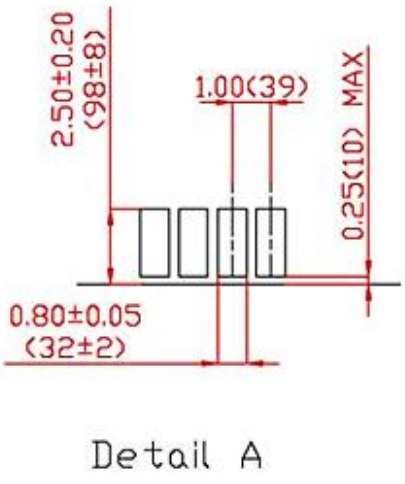
Values are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

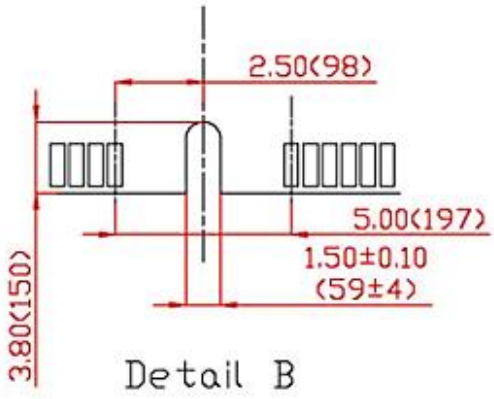
Parameter	Symbol	Data rate (Mbps)	1.5V Max.	Unit	Notes
Operating current (ACT-PRE)	IDDO	1600	880	mA	
Operating current (ACT-READ-PRE)	IDD1	1600	1120	mA	
Precharge power-down Standby current	IDD2P1	1600	288	mA	Fast PD Exit
	IDD2P0	1600	192	mA	Slow PD Exit
Precharge standby current	IDD2N	1600	448	mA	
Precharge standby current ODT current	IDD2NT	1600	512	mA	
Precharge quiet standby Current	IDD2Q	1600	416	mA	
Active power-down current (Always fast exit)	IDD3P	1600	384	mA	
Active standby current	IDD3N	1600	576	mA	
Operating current (Burst read operating)	IDD4R	1600	1680	mA	
Operating current (Burst write operating)	IDD4W	1600	1760	mA	
Burst refresh current	IDD5B	1600	4000	mA	
Self-refresh current Normal temperature range	IDD6	1600	192	mA	
Self-refresh current Extended temperature range	IDD6ET	1600	272	mA	
All bank interleave read current	IDD7	1600	3360	mA	
RESET low current	IDD8	1600	192	mA	

Module Dimensions

All dimensions are in millimeter(mils) and should be kept within a tolerance of ±0.15(6), unless otherwise specified.
1 pcs size: 133.35(5250) x 30.00(1181)







Change History			
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Rev. #	**Who**	**When**	**What**
01	Rik	2023-04-08	Initial version ;