力积存储
ZENTEL

Z6ABGH3DACA-QE

32 GB, 2Rx8 262-Pin DDR5-5600 SODIMM

Data Sheet

2023.06
Rev.01

32 GB DDR5 SDRAM SODIMM Specification

Specifications

Max. Speed; CAS Latency	DDR5-5600@CL=46
Row Cycle Time (tRCmin)	48 ns
Min. RAS-CAS-Delay (tRCD)	16 ns
Min. Row Precharge Time (tRP)	16 ns
Row Active Time (tRASmin)	32 ns
CL-tRCD-tRP	46-45-45
Operating Temperature	0 °C to +85 °C
Storage Temperature (T_{STG})	-55 °C to 100 °C

Features

- 262-pin, small-outline dual in-line memory module (SODIMM)
- 2Rx8 memory module (2 rank of x8 DDR5 SDRAMs)
- Power supply:
  - Vin_Bulk = 5V
  - VDD = VDDQ = 1.1 V (-33mV / +66mV)
  - VPP = 1.8V (–125mV / +250mV)
  - VDDSPD = 1.8V (1.7V to 1.98V)
- VrefDQ / VrefCA / VrefCS Training
- Burst Length (BL) 16 and 8 with Burst Chop(BC)
- On-DIMM SPD EEPROM with hub function and integrated temperature sensor (TS)
- On-DIMM Power management integrated circuit (PMIC)
- 32 internal banks; 8 groups of 4 banks each
- ZQ Calibration
- Gold edge contacts
- Fly-by topology
- Terminated control command and address bus
- PCB Height: 30.00 mm

Ordering Information

Part Number	*Module Density*	*Configuration*	*Speed Bin (CL-nRCD-nRP)*	*Operating Temperature*	*Storage Temperature*
Z6ABGH3DACA-QE	32 GB	2G × 64 (2Gx8 2Rank)	DDR5-5600 (46-45-45)	0℃~85 ℃	-55 ℃ ~100 ℃

Address Format

DIMM Density	*Row address*	*Column address*	*Device bank group address*	*Device bank address per group*	*Device configuration*	*Device Quantity*
32 GB(2Rx8,X64)	64K A[15:0]	1K A[9:0]	8 BG[1:0]	4 BA[1:0]	16Gb(2Gx8)	16

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Pin Configurations

Pin#	Front Side	Pin#	Front Side	Pin#	Front Side
1	VIN_BULK	89	VSS	175	CB3_B
3	VIN_BULK	91	DQ30	177	VSS
5	RFU	93	VSS	179	DQ0_B
7	PWR_GOOD	95	CB0_A	181	VSS
9	VSS	97	VSS	183	DQ2_B
11	DQ0 _A	99	CB2_A	185	VSS
13	VSS	101	VSS	187	DM0_B_n
15	DQ2_A	103	CB3_A	189	VSS
17	VSS	105	VSS	191	DQ4_B
19	DM0_A_n	107	CA0_A	193	VSS
21	VSS	109	CA1_A	195	DQ6_B
23	DQ4_A	111	VSS	197	VSS
25	VSS	113	CA2_A	199	DQ8_B
27	DQ6_A	115	CA4_A	201	VSS
29	VSS	117	VSS	203	DQ10_B
31	DQ8_A	119	CA6_A	205	VSS
33	VSS	121	CA8_A	207	DQS1_B_c
35	DQ10_A	123	VSS	209	DQS1_B_t
37	VSS	125	CA10_A	211	VSS
39	DQS1_A_c	KEY		213	DQ12_B
41	DQS1_A_t	127	CA12_A	215	VSS
43	VSS	129	VSS	217	DQ14_B
45	DQ12_A	131	CK0_A_t	219	VSS
47	VSS	133	CK1_A_c	221	DQ16_B
49	DQ14_A	135	VSS	223	VSS
51	VSS	137	CK0_B_t	225	DQ18_B
53	DQ16_A	139	CK0_B_c	227	VSS
55	VSS	141	VSS	229	DM2_B_n
57	DQ18_A	143	RFU	231	VSS
59	VSS	145	CA11_B	233	DQ20_B
61	DM2_A_n	147	VSS	235	VSS
63	VSS	149	CA9_B	237	DQ22_B
65	DQ20_A	151	CA7_B	239	VSS
67	VSS	153	VSS	241	DQ24_B
69	DQ22_A	155	CA5_B	243	VSS
71	VSS	157	CA3_B	245	DQ26_B
73	DQ24_A	159	VSS	247	VSS
75	VSS	161	CS0_B_N	249	DQS3_B_c
77	DQ26_A	163	RESET_n	251	DQS3_B_t
79	VSS	165	CS1_B_n	253	VSS
81	DQS3_A_c	167	VSS	255	DQ28_B
83	DQS4_A_t	169	DQS4_B_c	257	VSS
85	VSS	171	DQS4_B_t	259	DQ30_B
87	DQ28_A	173	VSS	261	VSS

Pin#	Back Side	Pin#	Back Side	Pin#	Back Side
2	HSA	90	VSS	176	CB2_B
4	HSCL	92	DQ31_A	178	VSS
6	HSDA	94	VSS	180	DQ1_B
8	PWR_EN	96	CB1_A	182	VSS
10	VSS	98	VSS	184	DQ3_B
12	DQ1_A	100	DQS4_A_c	186	VSS
14	VSS	102	DQS4_A_t	188	DQS0_B_c
16	DQ3_A	104	VSS	190	DQS0_B_t
18	VSS	106	CS0_A_n	192	VSS
20	DQS0_A_c	108	ALERT_n	194	DQ5_B
22	DQS0_A_t	110	CS1_A_n	196	VSS
24	VSS	112	VSS	198	DQ7_B
26	DQ5_A	114	CA3_A	200	VSS
28	VSS	116	CA5_A	202	DQ9_B
30	DQ7_A	118	VSS	204	VSS
32	VSS	120	CA7_A	206	DQ11_B
34	DQ09_A	122	CA9_A	208	VSS
36	VSS	124	VSS	210	DM1_B_n
38	DQ11_A	126	CA11_A	212	VSS
40	VSS	KEY		214	DQ13_B
42	DM1_A_n	128	RFU	216	VSS
44	VSS	130	VSS	218	DQ15_B
46	DQ13_A	132	CK1_A_t	220	VSS
48	VSS	134	CK1_A_c	222	DQ17_B
50	DQ15_A	136	VSS	224	VSS
52	VSS	138	CK1_B_t	226	DQ19_B
54	DQ17_A	140	CK1_B_c	228	VSS
56	VSS	142	VSS	230	DQS2_B_c
58	DQ19_A	144	CA12_B	232	DQS2_B_t
60	VSS	146	CA10_B	234	VSS
62	DQS2_A_c	148	VSS	236	DQ21_B
64	DQS2_A_t	150	CA8_B	238	VSS
66	VSS	152	CA6_B	240	DQ23_B
68	DQ21_A	154	VSS	242	VSS
70	VSS	156	CA4_B	244	DQ25_B
72	DA23_A	158	CA2_B	246	VSS
74	VSS	160	VSS	248	DQ27_B
76	DQ25_A	162	CA1_B	250	VSS
78	VSS	164	CA0_B	252	DM3_B_n
80	DQ27_A	166	VSS	254	VSS
82	VSS	168	CB0_B	256	DQ29_B
84	DM3_A_n	170	VSS	258	VSS
86	VSS	172	CB1_B	260	DQ31_B
88	DQ29_A	174	VSS	262	VSS

Pin Descriptions

Symbol	Type	Function
CKx_t, CKx_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA6_A, CA0_B - CA6_B	Input	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins mat not be interchanged between devices on the same bus.
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB3_A, CB0_B - CB3_B	Input	DIMM ECC check bits
DQS0_A_t - DQS4_A_t DQS0_A_c - DQS4_A_c DQS0_B_t - DQS4_B_t DQS0_B_c - DQS4_B_c	Input/ Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended
DM0_A_n-DM3_A_n, DM0_B_n-DM3_B_n	Input	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. DM is not supported for x4 device.
LBDQ	Output	Loopback Data Output: The Output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HiZ based on MR36:OP[2:0]
LBDQS	Output	Loopback Data Strobe: This is a single ended strobe with the Rising edge-aligned with Loopback data edge, falling edge aligned with data center. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or HIZ based on MR36:OP[2:0]
ALERT_n	Input/ Output	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	Host SidebandBus bus clock, supplied by the master.
HSDA	Input/ Output	Host SidebandBus data, connected from the master to bubs or host bus client devices.
HSA	Input	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C Basic address range.
RFU		Reserved for Future Use. No on DIMM electrical connection is present.

Symbol	Type	Function
PWR_EN	Input	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.
PWR_GOOD	Input/ Output	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or configured in the appropriate register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
VIN_BULK	Supply	5V power input supply to the PMIC for analog circuits.
VSS	Supply	Ground
NC		No connect: No internal electrical connection is present.
NF		No function: May have internal connection present, but has no function.

General Description

High-speed DDR5 SDRAM modules use DDR5 SDRAM devices with four or eight internal memory bank groups. DDR5 SDRAM modules benefit from DDR5 SDRAM's use of a 16n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR5 SDRAM effectively consists of a single 16n-bit-wide, eight-clock data transfer at the internal DRAM core and sixteen corresponding n-bit-wide, one-half-clockcycle data transfers at the I/O pins.
DDR5 modules use two sets of differential signals (DQS_t and DQS_c) to capture data, and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

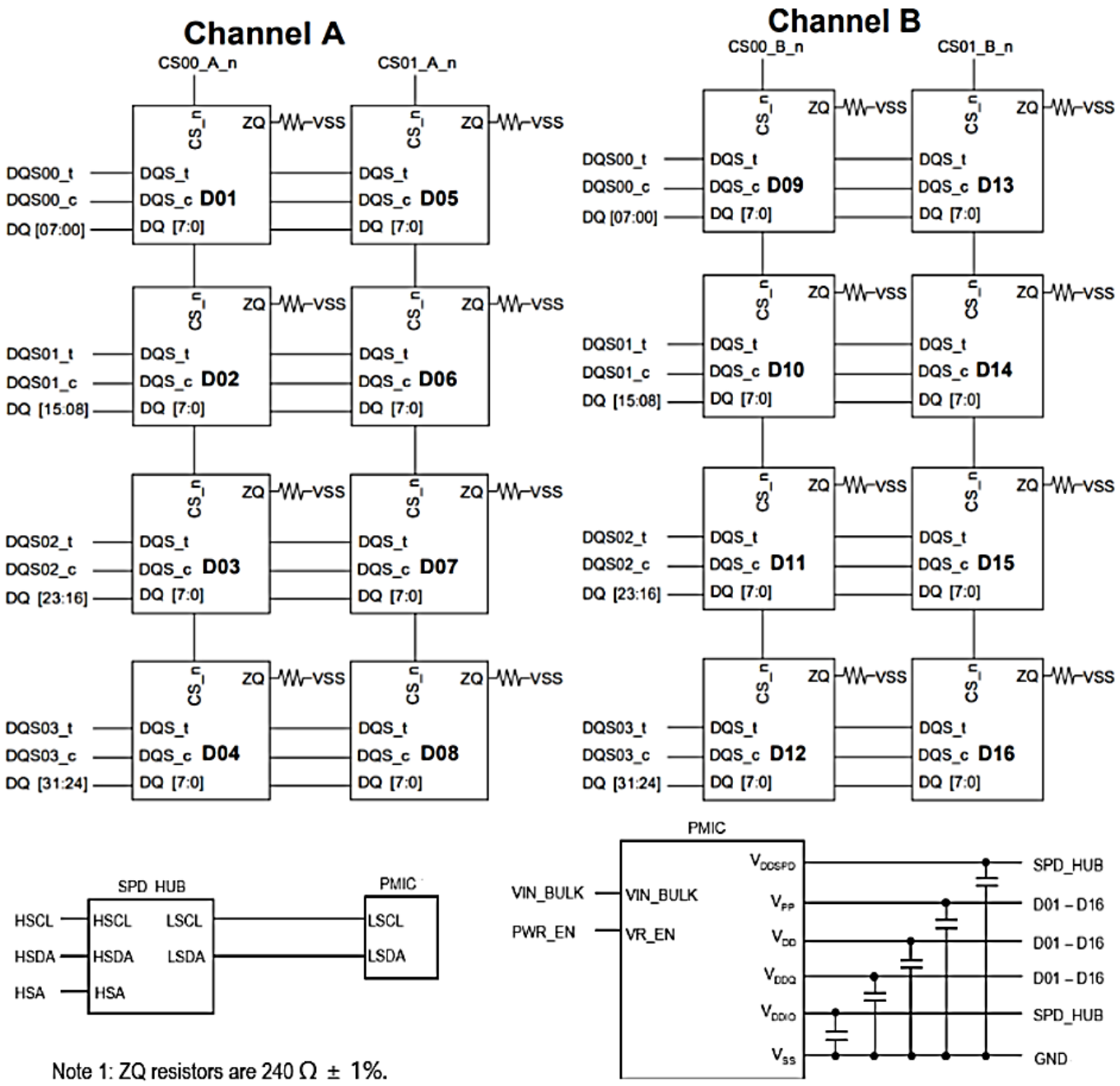
Power Management Integrated Circuit Operation

The power management integrated circuit (PMIC) is new for DDR5. For SODIMMs, JEDEC defines PMIC5100. This operation converts a 5V supply into regulated values for components on the module. The PMIC allows the host to monitor voltage and current via the sideband channel.
The PMIC5100 has one 5V nominal supply input pin from the card edge through VIN_Bulk. The PMIC has the ability to regulate lower voltages to the HUB which allows external access to read/configure this device prior to the VR ENABLE command. The VIN_Bulk supply, after the VR ENABLE command, will supply all regulated voltages to the PMIC and DRAM. By default, the PMIC powers up in I2C mode, and the host can reconfigure to support I3C-basic if needed.

SPD EEPROM HUB Operation

DDR5 SDRAM modules incorporate an SPD EEPROM with hub function with integrated thermal sensor (TS). The SPD data is stored in a 1024-byte including16 blocks (64 bytes per block), and each block may optionally be write-protected via software command.
The EEPROM resides on a two-wire I3C serial interface, which is also compatible with legacy I2C interface and is not integrated with the memory bus in any manner. It operates as an initiator/target device in the I3C-basic protocol, with all operations synchronized by the serial clock. Transfer rates of up to 12.5 MHz are achievable at 1.0V (NOM). The first 640 bytes are programmed by Zentel for DIMM parameters related usage. The remaining 384 bytes are available for the end user.
Zentel implements reversible software write protection on DDR5 SDRAM-based modules. This prevents the lower 640 bytes (bytes 0 to 639) from being inadvertently programmed or corrupted. The upper 384 bytes remain available for customer use and are unprotected

Function Block Diagram



Note 1: ZQ resistors are 240 Ω ± 1%.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.4	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.4	V	1
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 2.1	V	3
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA relative to Vss	-0.3 ~ 1.4	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

Note:
1. Stresses greater than those listed in this table may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage temperature is the case surface temperature on the center/top side of the device. For the measurement conditions, refer to JESD51-2 standard.
3. VPP must be equal or greater than VDD /VDDQ at all times during power on and operation of DRAM device.

DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Units	Grade	Note
		Min	Max			
T_{OPER_NORMAL}	Normal Operating Temperature	0	85	°C	NT	1,2,3,4
$T_{OPER\_EXTENDED}$	Extended Operating Temperature	0	95	°C	XT	1,2,3,4

Notes:
1. All operating temperature symbols, ranges, acronyms from JESD402-1.
2. Operating Temperature is the case surface temperature on the center / top side of the DRAM. For the measurement conditions, refer to JESD51-2.
3. All devices are required to operate in NT and XT temperature ranges.
4. When operating above 85°C, the host shall provide appropriate refresh mode controls associated with increased temperature range. The full description of these settings are defined in the tREFI parameters for REFab and REFsb command by device density table in the Refresh operations section (DRAM datasheet)

Operating Conditions

Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Host Supply Voltage	VIN_BULK	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	V_{DD}	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	V_{DDQ}	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	V_{PP}	1.746	1.8	1.908	V	3
PMIC Output Supply Voltage	VDDSPD	1.7	1.8	1.98	V	

Notes:

1. VDD must be within 66mv of VDDQ
2. AC parameters are measured with VDD and VDDQ tied together.
3. This includes all voltage noise from DC to 2 MHz at the DRAM package ball.

I_{DD}/I_{PP} Specifications and Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to **Table 302**; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,...(see **Table 302**); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 302**
IDDQ0	**Operating One Bank Active-Precharge IDDQ Current** **Same condition with IDD0,** however measuring IDDQ current instead of IDD current
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0,** however measuring IPP current instead of IDD current
IDD0F	**Operating Four Bank Active-Precharge Current** **External clock:** On; **tCK, nRC, nRAS, nRP, nRRD**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between ACT and PRE; **CA Inputs:** partially toggling according to **Table 303**; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with four bank active at a time: (see **Table 303**); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 303**
IDDQ0F	**Operating Four Bank Active-Precharge IDDQ Current** **Same condition with IDD0F,** however measuring IDDQ current instead of IDD current
IPP0F	**Operating Four Bank Active-Precharge IPP Current** **Same condition with IDD0F,** however measuring IPP current instead of IDD current
IDD2N	**Precharge Standby Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to **Table 304**; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 304**
IDDQ2N	**Precharge Standby IDDQ Current** **Same condition with IDD2N,** however measuring IDDQ current instead of IDD current
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N,** however measuring IPP current instead of IDD current
IDD2NT	**Precharge Standby Non-Target Command Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between WRITE commands; **CS_n, CA Inputs:** partially toggling according to **Table 305**; **Data IO:** VDDQ;**DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2];**Pattern Details:** see **Table 305**
IDDQ2NT (Optional)	**Precharge Standby Non-Target Command IDDQ Current** Same condition with IDD2NT, however measuring IDDQ current instead of IDD current
IPP2NT (Optional)	**Precharge Standby Non-Target Command IPP Current** Same condition with IDD2NT, however measuring IPP current instead of IDD current
IDD2P	**Precharge Power-Down** **Device in Precharge Power-Down, External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IDDQ current instead of IDD current
IPP2P	**Precharge Power-Down** **Same condition with IDD2P,** however measuring IPP current instead of IDD current
IDD3N	**Active Standby Current** **External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1; **CA Inputs:** partially toggling according to **Table 304**; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 304**
IDDQ3N	**Active Standby IDDQ Current** **Same condition with IDD3N,** however measuring IDDQ current instead of IDD current
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N,** however measuring IPP current instead of IDD current

IDD3P	**Active Power-Down Current** **Device in Active Power-Down, External clock:** On; **tCK**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **CS_n:** stable at 1 after Power Down Entry command; **CA Inputs:** stable at 1; CA11=H during the PDE command; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ3P	**Active Power-Down IDDQ Current** **Same condition with IDD3P,** however measuring IDDQ current instead of IDD current
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P,** however measuring IPP current instead of IDD current
IDD4R	**Operating Burst Read Current** **External clock:** On; **tCK, nCCD_S, CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between RD; **CA Inputs:** partially toggling according to **Table 306**; **Data IO:** seamless read data burst with different data between one burst and the next one according to **Table 306**; **DM_n:** stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see **Table 306**); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 306**
IDD4RC	**Operating Burst Read Current with Read CRC Read CRC enabled[4]. Other conditions:** see IDD4R
IDDQ4R	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R,** however measuring IPP current instead of IDD current
IDD4W	**Operating Burst Write Current** **External clock:** On; **tCK, nCCD_S_WR, CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** High between WR; **CA Inputs:** partially toggling according to **Table 307**; **Data IO:** seamless write data burst with different data between one burst and the next one according to **Table 307**; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see **Table 307**); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 307**
IDD4WC	**Operating Burst Write Current with Write CRC Write CRC enabled[3], Other conditions:** see IDD4W
IDDQ4W	**Operating Burst Write IDDQ Current** **Same condition with IDD4W,** however measuring IDDQ current instead of IDD current
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W,** however measuring IPP current instead of IDD current
IDD5B	**Burst Refresh Current (Normal Refresh Mode)** **External clock:** On; **tCK, nRFC**1: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to **Table 308**; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC1 (see **Table 308**); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 308**
IDDQ5B	**Burst Refresh IDDQ Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IDDQ current instead of IDD current
IPP5B	**Burst Refresh IPP Current (Normal Refresh Mode)** **Same condition with IDD5B,** however measuring IPP current instead of IDD current
IDD5F	**Burst Refresh Current (Fine Granularity Refresh Mode) tRFC=tRFC2, Other conditions: see IDD5B**
IDDQ5F	**Burst Refresh IDDQPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IDDQ current instead of IDD current
IPP5F	**Burst Refresh IPP Current (Fine Granularity Refresh Mode)** **Same condition with IDD5F,** however measuring IPP current instead of IDD current
IDD5C	**Burst Refresh Current (Same Bank Refresh Mode)** **External clock:** On; **tCK, nRFCsb**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between REF; **CA Inputs:** partially toggling according to **Table 309**; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFCsb (see **Table 309**); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 309**
IDDQ5C	**Burst Refresh IDDQPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IDDQ current instead of IDD current
IPP5C	**Burst Refresh IPP Current (Same Bank Refresh Mode)** **Same condition with IDD5C,** however measuring IPP current instead of IDD current

IDD6N	**Self Refresh Current: Normal Temperature Range** **TCASE:** 0 - 85°C; **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n#:** low; **CA, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** All ODT disabled in MR32-MR35;
IDDQ6N	**Self Refresh IDDQ Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IDDQ current instead of IDD current
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N,** however measuring IPP current instead of IDD current
IDD6E	**SelfRefresh Current: Extended Temperature Range**) **TCASE:** 85 - 95 °C; Extended[4]; **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n:** low; **CA, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]
IDDQ6E	**Self Refresh IDDQ Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IDDQ current instead of IDD current
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E,** however measuring IPP current instead of IDD current
IDD7	**Operating Bank Interleave Read Current** **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD_S, nFAW, tCCD_S CL**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n**: High between ACT and RDA; **CA Inputs:** partially toggling according to **Table 311**; **Data IO:** read data bursts with different data between one burst and the next one according to **Table 311**; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see **Table 311**; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Pattern Details:** see **Table 311**
IDDQ7	**Operating Bank Interleave Read IDDQ Current** **Same condition with IDD7,** however measuring IDDQ current instead of IDD current
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7,** however measuring IPP current instead of IDD current
IDD8	**Maximum Power Saving Deep Power Down Current** **External clock:** Off; **CK_t and CK_c**: HIGH; **tCK, nCPDED**: refer to Chapter 13.3 Timing Parameters by Speed Grade; **BL:** 16[1]; **CS_n#:** low; **CA:**High**, DM_n:** stable at 1; **Bank Activity:** All banks closed and device in MPSM deep power down mode5; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **Patterns Details**: same as IDD6N but MPSM is enabled in mode register.
IDDQ8	**Maximum Power Saving Deep Power Down IDDQ Current** **Same condition with IDD8,** however measuring IDDQ current instead of IDD current
IPP8	**Maximum Power Saving Deep Power Down IPP Current** **Same condition with IDD8,** however measuring IPP current instead of IDD current
IDD9 (Optional)	**MBIST Current** **Device in MBIST mode, External clock:** On; **CS_n**: Stable at 1 after MBIST entry; **CA Inputs:** stable at 1;**Data IO:** VDDQ; **Bank Activity:** MBIST operation; **Output Buffer and RTT:** Enabled in Mode Registers[2];
IDDQ9 (Optional)	**MBIST IDDQ Current** **Same condition with IDD9,** however measuring IDDQ current instead of IDD current
IPP9 (Optional)	**MBIST IPP Current** **Same condition with IDD9,** however measuring IPP current instead of IDD current

Notes:

1. Burst Length: BL16 fixed by MR0 OP[1:0]=00.
2. Output Buffer Enable
   - set MR5 OP[0] = 0] : Qoff = Output buffer enabled
   - set MR5 OP[2:1] = 00]: Pull-Up Output Driver Impedance Control = RZQ/7
   - set MR5 OP[7:6] = 00]: Pull-Down Output Driver Impedance Control = RZQ/7

   RTT_Nom enable
   - set MR35 OP[5:0] = 110110: RTT_NOM_WR = RTT_NOM_RD = RZQ/6 RTT_WR enable
   - set MR34 OP[5:3] = 010 RTT_WR = RZQ/2

   CA/CS/CK ODT, DQS_RTT_PART, and RTT_PARK disable
   - set MR32 OP[5:0] = 000000
   - set/MR33 OP[5:0] = 000000

- set MR34 OP[2:0] = 000

3. WRITE CRC enabled
   - set MR50 OP[2:1] = 11
4. Read CRC enabled
   - set MR50:OP[0]=1
5. MPSM Deep Power Down Mode
   - set MR2:OP[3]=1 if PDA Enumerate ID not equal to 15
   - set MR2:OP[5]=1 if PDA Enumerate ID equal to 15

Tel：0579-81088899

I_{DD} Specification

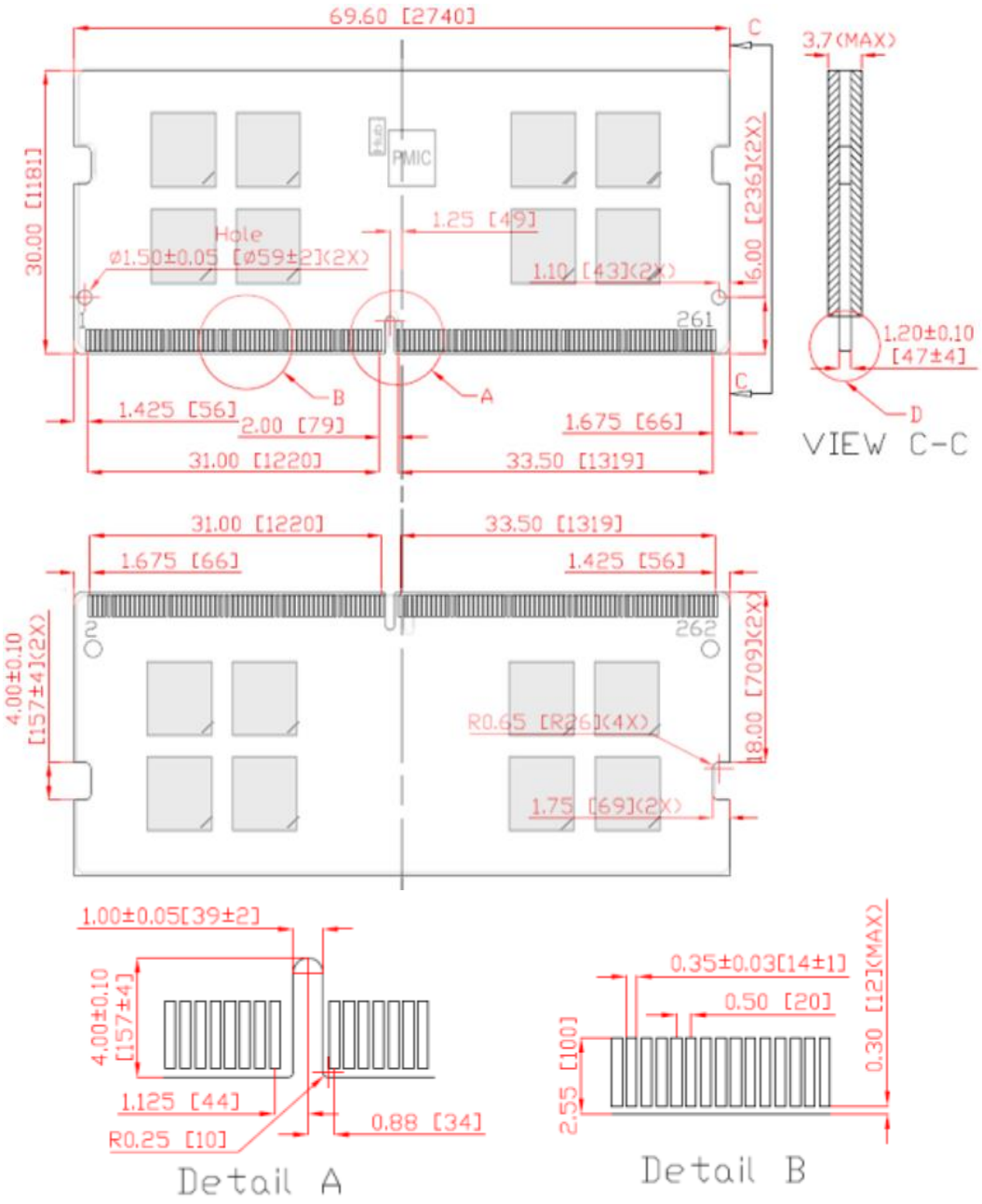
Product Type	Z6ABGH3DACA-QE	Unit	Note
Organization	32 GB		
	2 Rank (X8)		
	X64		
Symbol	Current		
IDD0	1004.8	mA	
IDD0F	1552	mA	
IDD2N	816	mA	
IDD2NT	1313.6	mA	
IDD2P	689.6	mA	
IDD3N	1920	mA	
IDD3P	1792	mA	
IDD4R	4403.2	mA	
IDD4RC	4288	mA	
IDD4W	5008	mA	
IDD4WC	4880	mA	
IDD5B	3664	mA	
IDD5F	3435.2	mA	
IDD5FC	1712	mA	
IDD6E	820.8	mA	
IDD7	4992	mA	
IDD8	416	mA	
IDD9	3014.4	mA	

I_{PP} Specification

Product Type	Z6ABGH3DACA-QE	Unit	Note
Organization	32 GB		
	2 Rank (X8)		
	X64		
Symbol	Current		
IPP0	110.4	mA	
IPP0F	224	mA	
IPP2N	64	mA	
IPP2NT	64	mA	
IPP2P	56	mA	
IPP3N	238.4	mA	
IPP3P	220.8	mA	
IPP4R	288	mA	
IPP4W	329.6	mA	
IPP5B	720	mA	
IPP5F	720	mA	
IPP5C	720	mA	
IPP6E	136	mA	
IPP7	844.8	mA	
IPP8	56	mA	
IPP9	480	mA	

Module Dimensions

All dimensions are in millimeter[mils] and should be kept within a tolerance of +/- 0.15[6], unless otherwise specified.



Change History			
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Rev. #	**Who**	**When**	**What**
01	Rik	2023-06-08	Initial version