力积存储
ZENTEL

Z6F4GH4SCCA-MC

4 GB, 1Rx16 260-Pin DDR4-3200 SODIMM

Data Sheet

2023.05
Rev.01

4 GB DDR4 SDRAM SODIMM Specification

Specifications

Max. Speed; CAS Latency	DDR4-3200@CL=22
Row Cycle Time (tRCmin)	45.75 ns
Refresh to Active/Refresh Command Time (tRFCmin)	350 ns
RAS-CAS-Delay (tRCD min)	13.75 ns
Row Precharge Time (tRP min)	13.75 ns
Row Active Time (tRASmin)	32 ns
Operating Temperature	0 °C to +85 °C
Storage Temperature (T_{STG})	-55 °C to 100 °C

Features

- 260-pin, small-outline dual in-line memory module (SODIMM)
- 1Rx16 memory module (1 rank of x16 DDR4 SDRAMs)
- Power supply:
  - VDD = VDDQ = 1.2 V ± 5%
  - VPP = 2.5 V –5%/+10%
  - VDDSPD = 2.2 V to 3.6 V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die VREFDQ generation and calibration
- On-board I^2C serial presence-detect (SPD) EEPROM
- 8 internal banks; 2 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Fly-by topology
- Terminated control command and address bus
- PCB Height: 1.18” (30.00 mm)

Address Format

DIMM Density	*Row address*	*Column address*	*Device bank group address*	*Device bank address per group*	*Device configuration*	*Module rank address*	*Device Quantity*
4GB(1Rx16,X64)	64K A[15:0]	1K A[9:0]	1 BG[1:0]	4 BA[1:0]	8Gb(512Mx16)	1 CS_n[0]	4

Pin Configurations

Pin #	Front	Pin #	Front	Pin #	Front	Pin #	Back	Pin #	Back	Pin #	Back
1	VSS	2	VSS	89	VSS	90	VSS	175	VSS	176	VSS
3	DQ5	4	DQ4	91	CB1, NC	92	CB0, NC	177	DQS4_c	178	DM4_n/DBI4_n
5	VSS	6	VSS	93	VSS	94	VSS	179	DQS4_t	180	VSS
7	DQ1	8	DQ0	95	DQS8_c	96	DM8_n/DBI8_n	181	VSS	182	DQ39
9	VSS	10	VSS	97	DQS8_t	98	VSS	183	DQ38	184	VSS
11	DQS0_c	12	DM0_n/DBI0_n	99	VSS	100	CB6, NC	185	VSS	186	DQ35
13	DQS0_t	14	VSS	101	CB2, NC	102	VSS	187	DQ34	188	VSS
15	VSS	16	DQ6	103	VSS	104	CB7, NC	189	VSS	190	DQ45
17	DQ7	18	VSS	105	CB3, NC	106	VSS	191	DQ44	192	VSS
19	VSS	20	DQ2	107	VSS	108	RESET_n	193	VSS	194	DQ41
21	DQ3	22	VSS	109	CKE0	110	CKE1	195	DQ40	196	VSS
23	VSS	24	DQ12	111	VDD	112	VDD	197	VSS	198	DQS5_c
25	DQ13	26	VSS	113	BG1	114	ACT_n	199	DM5_n/DBI5_n	200	DQS5_t
27	VSS	28	DQ8	115	BG0	116	ALERT_n	201	VSS	202	VSS
29	DQ9	30	VSS	117	VDD	118	VDD	203	DQ46	204	DQ47
31	VSS	32	DQS1_c	119	A12	120	A11	205	VSS	206	VSS
33	DM1_n/DBI1_n	34	DQS1_t	121	A9	122	A7	207	DQ42	208	DQ43
35	VSS	36	VSS	123	VDD	124	VDD	209	VSS	210	VSS
37	DQ15	38	DQ14	125	A8	126	A5	211	DQ52	212	DQ53
39	VSS	40	VSS	127	A6	128	A4	213	VSS	214	VSS
41	DQ10	42	DQ11	129	VDD	130	VDD	215	DQ49	216	DQ48
43	VSS	44	VSS	131	A3	132	A2	217	VSS	218	VSS
45	DQ21	46	DQ20	133	A1	134	EVENT_n	219	DQS6_c	220	DM6_n/DBI6_n
47	VSS	48	VSS	135	VDD	136	VDD	221	DQS6_t	222	VSS
49	DQ17	50	DQ16	137	CK0_t	138	CK1_t	223	VSS	224	DQ54
51	VSS	52	VSS	139	CK0_c	140	CK1_c	225	DQ55	226	VSS
53	DQS2_c	54	DM2_n/DBI2_n	141	VDD	142	VDD	227	VSS	228	DQ50
55	DQS2_t	56	VSS	KEY		KEY		229	DQ51	230	VSS
57	VSS	58	DQ22	143	PARITY	144	A0	231	VSS	232	DQ60
59	DQ23	60	VSS	145	BA1	146	A10/AP	233	DQ61	234	VSS

Pin#	Front	Pin#	Front	Pin #	Front	Pin#	Back	Pin#	Back	Pin#	Back
61	VSS	62	DQ18	147	VDD	148	VDD	235	VSS	236	DQ57
63	DQ19	64	VSS	149	CS0_n	150	BA0	237	DQ56	238	VSS
65	VSS	66	DQ28	151	A14/WE_ n	152	A16/RAS_ n	239	VSS	240	DQS7_ c
67	DQ29	68	VSS	153	VDD	154	VDD	241	DM7_n/D BI7_n	242	DQS7_ t
69	VSS	70	DQ24	155	ODT0	156	A15/CAS_ n	243	VSS	244	VSS
71	DQ25	72	VSS	157	CS1_n	158	A13	245	DQ62	246	DQ63
73	VSS	74	DQS3_c	159	VDD	160	VDD	247	VSS	248	VSS
75	DM3_n/D BI3_n	76	DQS3_t	161	ODT1	162	C0, CS2_n, NC	249	DQ58	250	DQ59
77	VSS	78	VSS	163	VDD	164	VREFCA	251	VSS	252	VSS
79	DQ30	80	DQ31	165	C1, CS3_n, NC	166	SA2	253	SCL	254	SDA
81	VSS	82	VSS	167	VSS	168	VSS	255	VDDSPD	256	SA0
83	DQ26	84	DQ27	169	DQ37	170	DQ36	257	VPP	258	VTT
85	VSS	86	VSS	171	VSS	172	VSS	259	VPP	260	SA1
87	CB5, NC	88	CB4, NC	173	DQ33	174	DQ32				

Pin Descriptions

Symbol	Type	Function
CKx_t, CKx_c,	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKEx	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CSx_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code
Cx	Input	Chip ID: Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODTx	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/A15. WE_n/A14.	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table
BGx	Input	Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle
BAx	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle
Ax	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses
A12/BC_n	Input	Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-thefly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
Parity	Input	Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n Low
SAx	Input	Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus.
SCL	Input	Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus

Symbol	Type	Function
RESET_n	CMOS Input	Active Low Asynchronous Reset: Reset is active when RESET_n is Low, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation
DQx, CBx	I/O	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used
DQSx_t-DQSx_c	I/O	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIL_n)	I/O	Input data mask and data bus inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for SODIMMs).
SDA	I/O	Serial Data: Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input.
EVENT_n	Output	Temperature event: The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	Termination data strobe: When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component datasheet (TDQS_t and TDQS_c are not valid for SODIMMs).
VDD	Supply	Module power supply: 1.2V (TYP).
VPP	Supply	DRAM activating power supply: 2.5V –0.125V / +0.250V.
VREFCA	Supply	Reference voltage for control, command, and address pins.
VSS	Supply	Ground
VTT	Supply	Power supply for termination of address, command, and control VDD/2.
VDDSPD	Supply	Power supply used to power the I2C bus for SPD
RFU	-	Reserved for Future Use: No on DIMM electrical connection is present
NC	-	No Connect: No on DIMM electrical connection is present

General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing a total of 16 banks. Sixteen-bit-wide DDR4 SDRAM has 2 internal bank groups consisting of 4 memory banks each, providing a total of 8 banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8n-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. DDR4 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

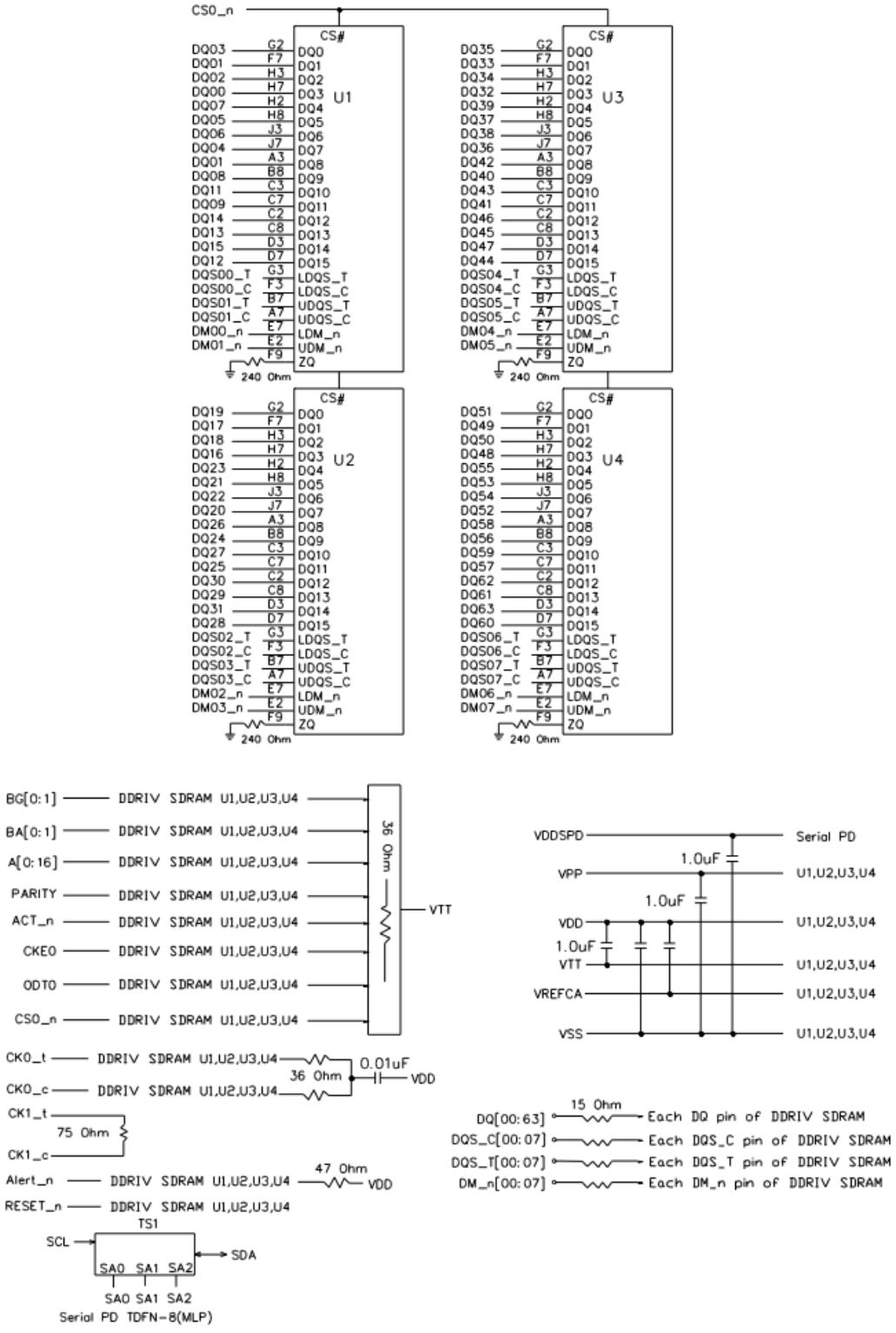
Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

Serial Presence-Detect EEPROM Operation

DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte EEPROM. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM’s SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

Function Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note
VDD	Voltage on VDD pin relative to Vss	-0.4 ~ 1.5	V	
VDDQ	Voltage on VDDQ pin relative to Vss	-0.4 ~ 1.5	V	
VPP	Voltage on VPP pin relative to Vss	-0.4 ~ 3.0	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.4 ~ 1.5	V	
T_{STG}	Storage Temperature	-55 to +100	ºC	

Note: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Note
		Min	Max		
T_{CASE}	Operating Temperature	0	95	ºC	1,2,3,4

Notes:
1. Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2. The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 ºC under all other specification parameters.
3. Above 85 °C the Auto-Refresh command interval has to be reduced to tREFI= 3.9 µs
4. When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”.

Operating Conditions

Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.14	1.2	1.26	V	1,2,3
Supply Voltage for Output	V_{DDQ}	1.14	1.2	1.26	V	1,2,3
Peak-to-Peak Voltage	V_{PP}	2.375	2.5	2.75	V	3
Reference Voltage for ADD, CMD inputs	V_{REF}	0.49 ×V_{DD}	0.5 ×V_{DDQ}	0.51 ×V_{DD}	V	

Notes:

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

Single-ended AC & DC input levels for Command and Address

Parameter	Symbol	Min.	Max.	Unit
$V_{IH.CA}$(DC65)	DC input logic high	V_{REFCA} + 0.065	V_{DD}	V
$V_{IL.CA}$(DC65)	DC input logic low	V_{SS}	V_{REFCA}-0.065	V
$V_{IH.CA}$(AC90)	AC input logic high	V_{SS}+0.09		V
$V_{IL.CA}$(AC90)	AC input logic low		V_{REF}-0.09	V

I_{DD}/I_{PP} Specifications and Conditions

Symbol	Description
IDD0 IPP0	Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD1 IPP1	Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2N IPP2N	Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern
IDD2P IPP2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD3N IPP3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern
IDD3P IPP3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0
IDD4R IPP4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[2] ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD4W IPP4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks:

Symbol	Description
	0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5B IPP5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD5F2 IPP5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2,
IDD5F4 IPP5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4,
IDD6N IPP6N	Self Refresh Current: Normal Temperature Range Tcase: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MIDLEVEL
IDD6E IPP6E	Self-Refresh Current: Extended Temperature Range) TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2]; ODT Signal: MID-LEVEL
IDD6R IPP6R	Self-Refresh Current: Reduced Temperature Range TCase: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced[4] ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: MID-LEVEL
IDD6A IPP6A	Auto Self-Refresh Current TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto[4] ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: MID-LEVEL
IDD7 IPP7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 8[1] ; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[2] ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern
IDD8 IPP8	Maximum Power Down Current TBD

Notes:

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable - set MR1 [A12 = 0] : Qoff = Output buffer enabled - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7 RTT_Nom enable - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6 RTT_WR enable - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2 RTT_PARK disable - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s 010] : 1866MT/s, 2133MT/s 011] : 2400MT/s Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate DLL disabled : set MR1 [A0 = 0] CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s 010] : 2400MT/s Read DBI enabled : set MR5 [A12 = 1] Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal 01] : Reduced Temperature range 10] : Extended Temperature range 11] : Auto Self Refresh

I_{DD} Specification

Product Type	Z6F4GH4SCAA-MC	Unit	Note
Organization	4GB		
	1 Rank (X16)		
	X64		
Symbol	Current		
IDD0	180	mA	2
IDD1	232	mA	2
IDD2N	120	mA	3
IDD2NT	140	mA	2
IDD2P	84	mA	3
IDD2Q	100	mA	3
IDD3N	132	mA	3
IDD3P	104	mA	3
IDD4R	844	mA	2
IDD4W	700	mA	2
IDD5B	816	mA	2
IDD5F2	588	mA	2
IDD5F4	528	mA	2
IDD6N	84	mA	3
IDD6E	112	mA	3
IDD6R	56	mA	3
IDD6A	112	mA	3
IDD7	788	mA	2
IDD8	48	mA	3

Notes:
1. Calculated values from Device data.
2. One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
3. All ranks in this IDD/IPP condition

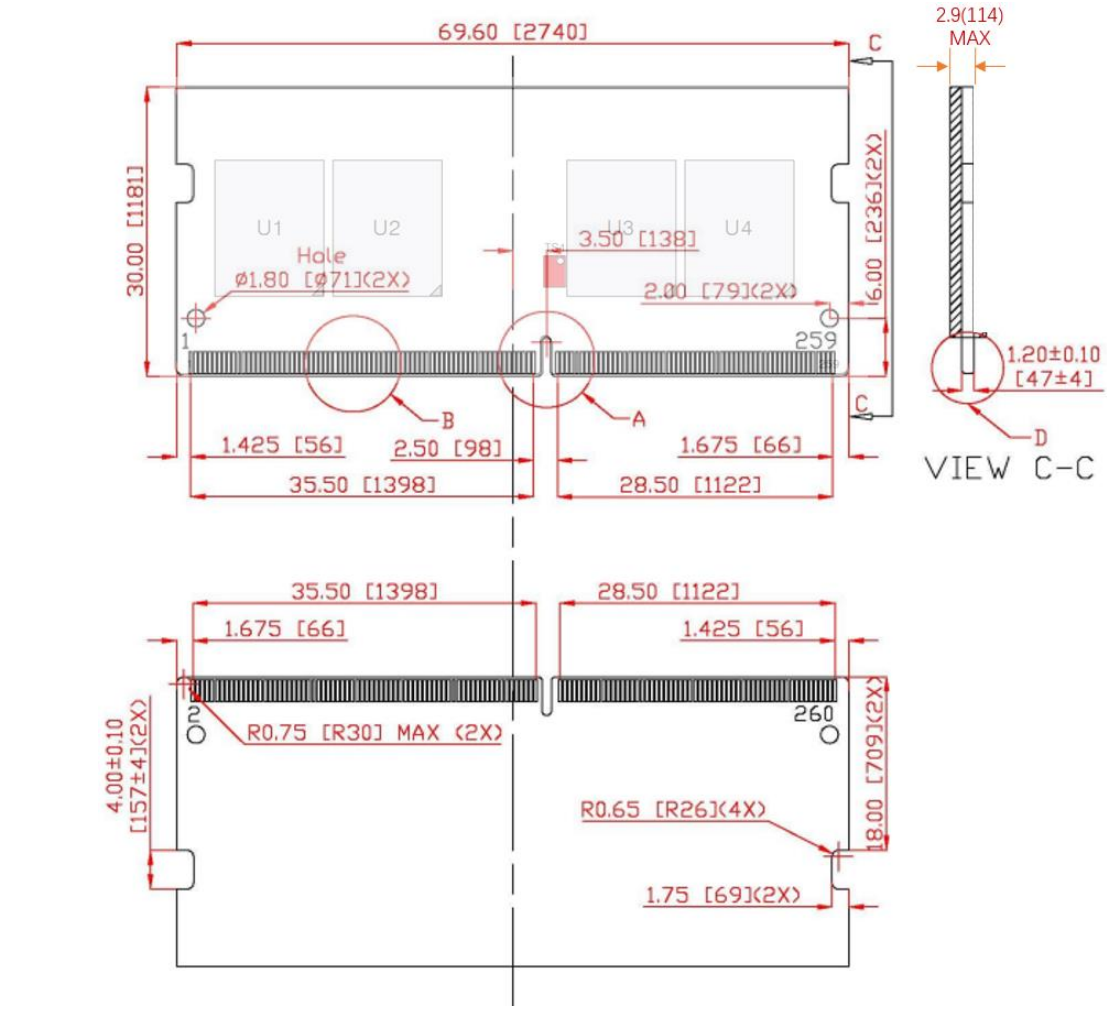
I_{PP} Specification

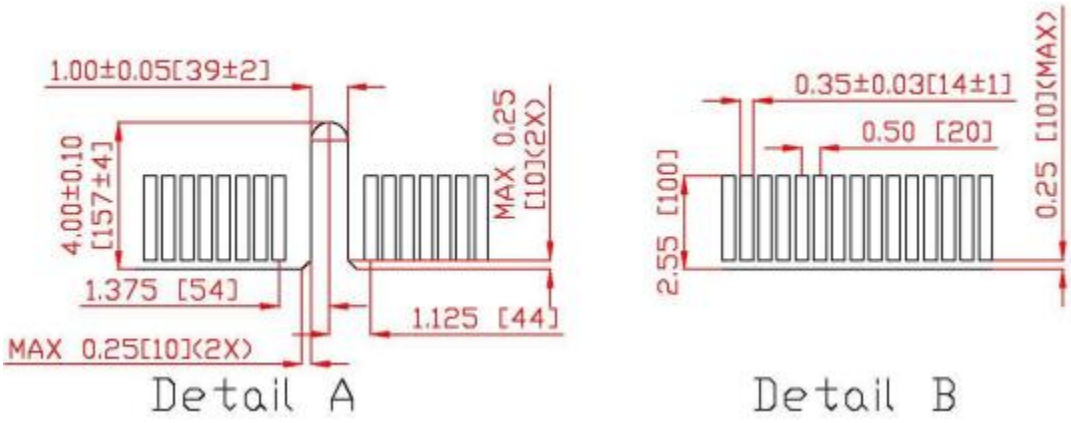
Product Type	Z6F4GH4SCAA-MC	Unit	Note
Organization	4GB		
	1 Rank (X16)		
	X64		
Symbol	Current		
IPP0	34.4	mA	2
IPP1	38.8	mA	2
IPP2N	12.8	mA	3
IPP2P	12	mA	3
IPP3N	64	mA	3
IPP3P	64	mA	3
IPP4R	88	mA	2
IPP4W	88	mA	2
IPP5B	244	mA	2
IPP6N	160	mA	3
IPP6E	132	mA	3
IPP6R	20	mA	3
IPP6A	28	mA	3
IPP7	96	mA	2
IPP8	12.8	mA	3

Notes:
1. Calculated values from Device data.
2. One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
3. All ranks in this IDD/IPP condition

Module Dimensions

All dimensions are in millimeter[mils] and should be kept within a tolerance of +/- 0.15[6], unless otherwise specified.





Change History			
Document No.: DSZ6F4GH4SCCAZF.(Rev.#)			
Rev. #	**Who**	**When**	**What**
01	SAE	2023-05-31	Initial version ;