8 GB DDR3 SDRAM SODIMM Specification

Specifications

Max. Speed	DDR3-1333
Fast Data Transfer Rates	PC3-10600
tCK (min) (ns)	1.5
CAS Latency (nCK)	9
tRCD (min) (nCK)	9
tRP (min) (nCK)	9
tRAS (min) (ns)	36
tRC (min) (ns)	49.5
CL-tRCD-tRP	9-9-9
Operating Temperature (º C)	0 to +70

Features

- DDR3 functionality and operations supported as defined in the component data sheet
- 204-pin, small-outline dual in-line memory module (SODIMM)
- 2Rx8 memory module (2 rank of x8 DDR3 SDRAMs)
- Power supply:
  - VDD = 1.5V(1.425~1.575V)
  - VDDSPD = 3.0 V to 3.6 V
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- On-board I^2C serial presence-detect (SPD) EEPROM
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Fly-by topology
- Module height: 1.181” (30.00 mm)
- Gold edge contacts
- Terminated control, command, and address bus

Pin Assignments (Front side/back side)

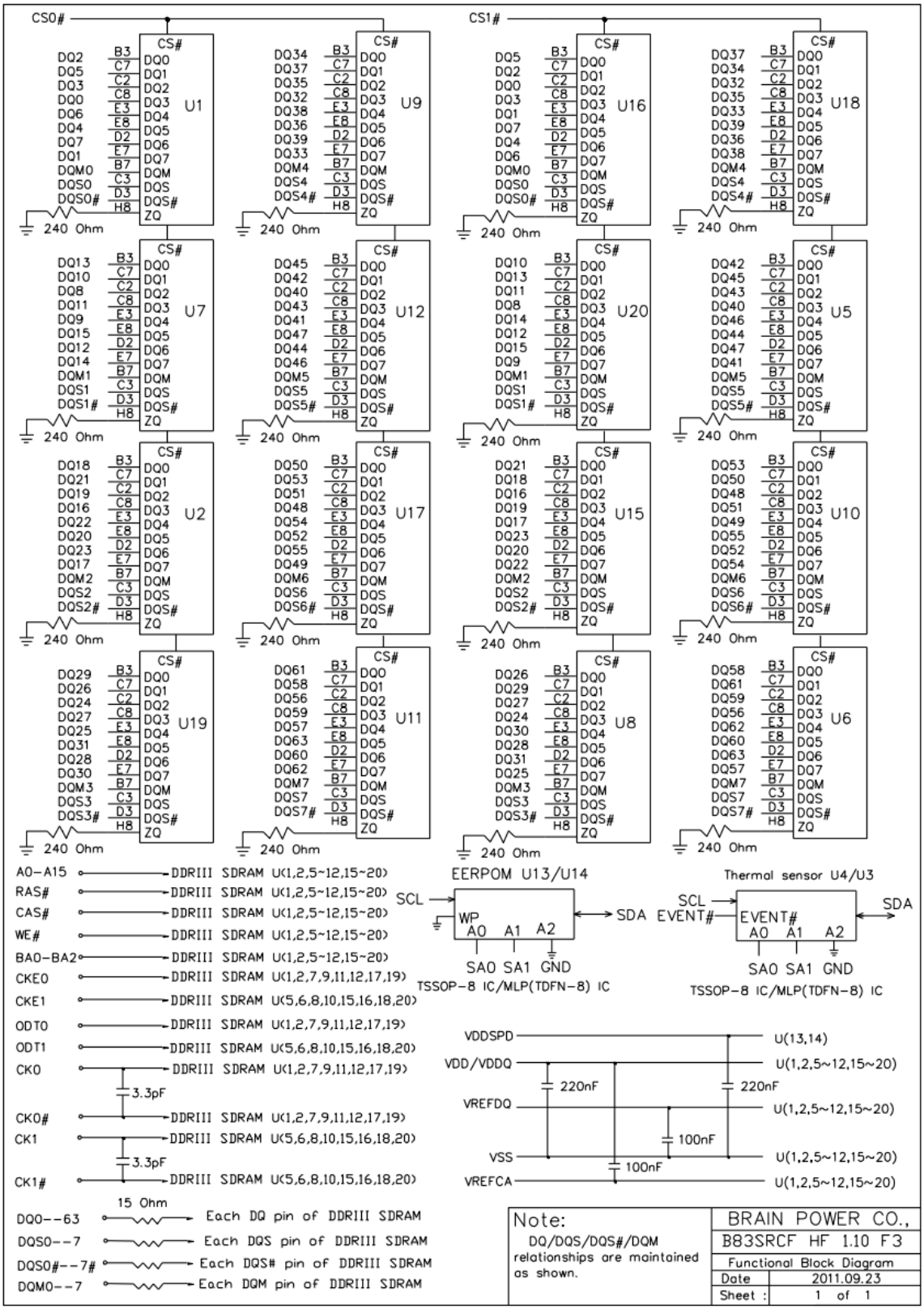
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	2	VSS	69	DQ27	70	DQ31	137	DQS4	138	VSS
3	VSS	4	DQ4	71	VSS	72	VSS	139	VSS	140	DQ38
5	DQ0	6	DQ5	73	CKE0	74	NC,CKE1	141	DQ34	142	DQ39
7	DQ1	8	VSS	75	VDD	76	VDD	143	DQ35	144	VSS
9	VSS	10	DQS0#	77	NC	78	A15	145	VSS	146	DQ44
11	DM0	12	DQS0	79	BA2	80	A14	147	DQ40	148	DQ45
13	VSS	14	VSS	81	VDD	82	VDD	149	DQ41	150	VSS
15	DQ2	16	DQ6	83	A12/BC#	84	A11	151	VSS	152	DQS5#
17	DQ3	18	DQ7	85	A9	86	A7	153	DM5	154	DQS5
19	VSS	20	VSS	87	VDD	88	VDD	155	VSS	156	VSS
21	DQ8	22	DQ12	89	A8	90	A6	157	DQ42	158	DQ46
23	DQ9	24	DQ13	91	A5	92	A4	159	DQ43	160	DQ47
25	VSS	26	VSS	93	VDD	94	VDD	161	VSS	162	VSS
27	DQS1#	28	DM1	95	A3	96	A2	163	DQ48	164	DQ52
29	DQS1	30	RESET#	97	A1	98	A0	165	DQ49	166	DQ53
31	VSS	32	VSS	99	VDD	100	VDD	167	VSS	168	VSS
33	DQ10	34	DQ14	101	CK0	102	CK1	169	DQS6#	170	DM6
35	DQ11	36	DQ15	103	CK0#	104	CK1#	171	DQS6	172	VSS
37	VSS	38	VSS	105	VDD	106	VDD	173	VSS	174	DQ54
39	DQ16	40	DQ20	107	A10/AP	108	BA1	175	DQ50	176	DQ55
41	DQ17	42	DQ21	109	BA0	110	RAS#	177	DQ51	178	VSS
43	VSS	44	VSS	111	VDD	112	VDD	179	VSS	180	DQ60
45	DQS2#	46	DM2	113	WE#	114	S0#	181	DQ56	182	DQ61
47	DQS2	48	VSS	115	CAS#	116	ODT0	183	DQ57	184	VSS
49	VSS	50	DQ22	117	VDD	118	VDD	185	VSS	186	DQS7#
51	DQ18	52	DQ23	119	A13	120	NC,ODT1	187	DM7	188	DQS7
53	DQ19	54	VSS	121	NC,S1#	122	NC	189	VSS	190	VSS
55	VSS	56	DQ28	123	VDD	124	VDD	191	DQ58	192	DQ62
57	DQ24	58	DQ29	125	TEST	126	VREFCA	193	DQ59	194	DQ63
59	DQ25	60	VSS	127	VSS	128	VSS	195	VSS	196	VSS
61	VSS	62	DQS3#	129	DQ32	130	DQ36	197	SA0	198	EVENT#
63	DM3	64	DQS3	131	DQ33	132	DQ37	199	VDDSPD	200	SDA
65	VSS	66	VSS	133	VSS	134	VSS	201	SA1	202	DCL
67	DQ26	68	DQ30	135	DQS4#	136	DM4	203	VTT	204	VTT

Pin Descriptions

Pin Name	Function
A0~A15	SDRAM address bus
BA0~BA2	SDRAM bank select
RAS#	SDRAM row address strobe
CAS#	SDRAM column address strobe
WE#	SDRAM write enable
S0#	DIMM Rank Select Lines
CKE0	SDRAM clock enable lines
ODT0	On-die termination control lines
DQ0-DQ63	DIMM memory data bus
DQS0~DQS7	SDRAM data strobes(positive line of differential pair)
DQS0#~DQS7#	SDRAM data strobes(negative line of differential pair)
DM0 ~DM7	SDRAM data masks high data strobes(x8-based X64 DIMMs)
CK0-CK1	SDRAM clocks(positive line of differential pair)
CK0#-CK1#	SDRAM clocks(negative line of differential pair)
SCL	I^2C serial bus clock for EEPROM
SDA	I^2C serial bus data line for EEPROM
SA0-SA1	I^2C slave address select for EEPROM
VDD*	SDRAM core power supply
VDDQ*	SDRAM I/0 Driver power supply
VREFDQ	SDRAM I/O reference supply
VREFCA	SDRAM command/address reference supply
VSS	Power supply return(ground)
VDDSPD	Serial EEPROM positive power supply
NC	Spare pins(no connect)
TEST	Used by memory bus analysis tools(unused on memory DIMMS)
RESET	Set DRAMs to Known State
NF	No function
VTT	SDRAM I/O termination supply
RSVD	Reserved for future use
EVENT#	An output of the thermal sensor to indicate critical module temperature

*VDD and VDDQ pins are tied common to a single power-plane on these designs.

Functional Diagram



General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins. DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

Serial Presence-Detect EEPROM Operation

The 2K-bit Serial Presence Detect (SPD) EEPROM is fully compatible to industrial standard I2C/SMBus interface and compliant to the JEDEC 42.4 specification. The EEPROM memory is organized as 256 x 8 bits. This is designed for memory module applications in most PC and Server platforms, as well as other related applications. The EEPROM operates from 1.7V to 3.6V and is offered in 8-pin Ultra-thin DFN package, 2 mm x 3 mm x 0.6 mm (max.), which is lead-free, RoHS, halogen free or Green compliance, providing space as well as cost saving for DIMM manufactures.

One of the features is to permanently lock the data in its first half (lower) 128 bytes (address 00h to 7Fh). This feature is specifically designed for use in DRAM DIMM with SPD. All information concerning the DRAM module configuration (e.g. access speed, size, and organization) can be kept write-protected in the first half of the memory. The second half (upper) 128 bytes of the memory (address 80h to FFh) can't be write-protected using two different software write protection mechanisms. By sending a specified sequence to the device, the first 128 bytes memory can be write-protected either permanently or resettable. The operating ambient temperature range is from -40°C to +85°C.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.975	V	1, 2
Power supply voltage for output	VDDQ	-0.4 to +1.975	V	1, 2
Input voltage	VIN	-0.4 to +1.975	V	1
Output voltage	VOUT	-0.4 to +1.975	V	1

Notes:

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions for DDR3 (1.5V)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Supply voltage	VDD	1.425	1.5	1.575	V	1, 2
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1, 2
Input reference voltage command/address bus	VREFCA(DC)	0.49*VDD	0.5*VDD	0.51*VDD	V	
I/O reference voltage DQ bus	VREFDQ(DC)	0.49*VDD	0.5*VDD	0.51*VDD	V	
Module ambient operating temperature	TA	0	-	70	°C	3
DDR3 SDRAM component case operating temperature	TC	0	-	95	°C	4

Notes:

1. If minimum limit is exceeded, input levels shall be governed by DDR3 specifications.
2. Under 1.5V operation, the DDR3 device operates to the DDR3 specification under the same speed timings as defined for this device.
3. TA and TC are simultaneous requirements.
4. The refresh rate is required to double when 85°C < TC ≤ 95°C.

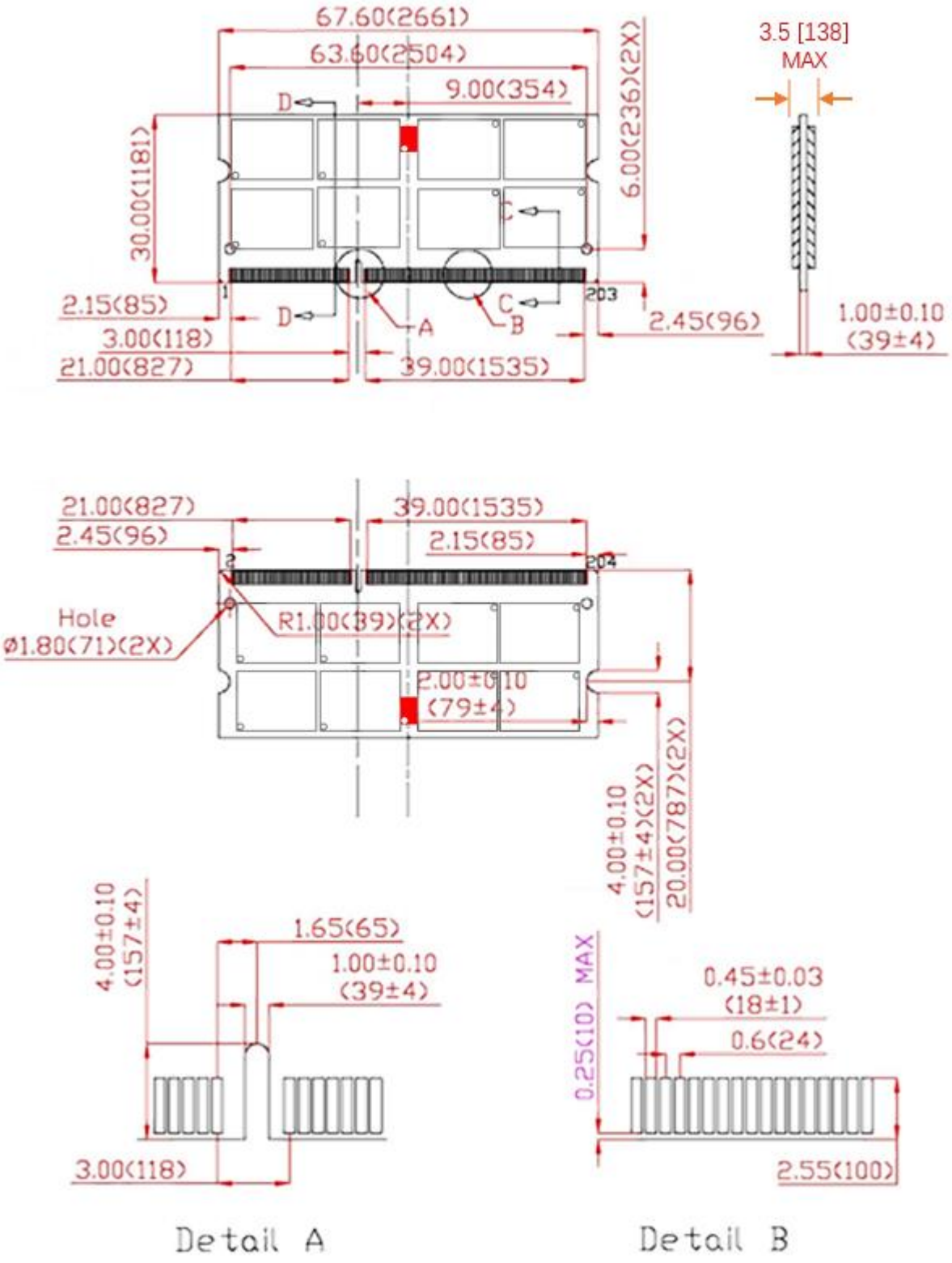
IDD Specifications

Values are computed from values specified in the 4Gb (512 Meg x 8) component data sheet

Parameter	Symbol	Data rate (Mbps)	1.5V Max.	Unit	Notes
Operating current (ACT-PRE)	IDDO	1333	816	mA	
Operating current (ACT-READ-PRE)	IDD1	1333	1168	mA	
Precharge power-down Standby current	IDD2P1	1333	1168	mA	Fast PD Exit
	IDD2P0	1333	1136	mA	Slow PD Exit
Precharge standby current	IDD2N	1333	80	mA	
Precharge standby current ODT current	IDD2NT	1333	80	mA	
Precharge quiet standby Current	IDD2Q	1333	80	mA	
Active power-down current (Always fast exit)	IDD3P	1333	336	mA	
Active standby current	IDD3N	1333	352	mA	
Operating current (Burst read operating)	IDD4R	1333	1920	mA	
Operating current (Burst write operating)	IDD4W	1333	2128	mA	
Burst refresh current	IDD5B	1333	416	mA	
Self-refresh current Normal temperature range	IDD6	1333	2256	mA	
Self-refresh current Extended temperature range	IDD6ET	1333	2384	mA	
All bank interleave read current	IDD7	1333	3152	mA	
RESET low current	IDD8	1333	352	mA	

Module Dimensions

All dimensions are in millimeter(mils) and should be kept within a tolerance of ±0.15(6), unless otherwise specified.
1 pcs size: 67.60(2661) x 30.00(1181)



Change History			
Doc. No.: DSZ6T8GZ3DACAZF.(Rev.#)			
Rev. #	**Who**	**When**	**What**
01	Rik	2023-03-10	Initial version derived from DSA6T4GF3SACAHPF.01; Updated Specifications, IDD Specifications